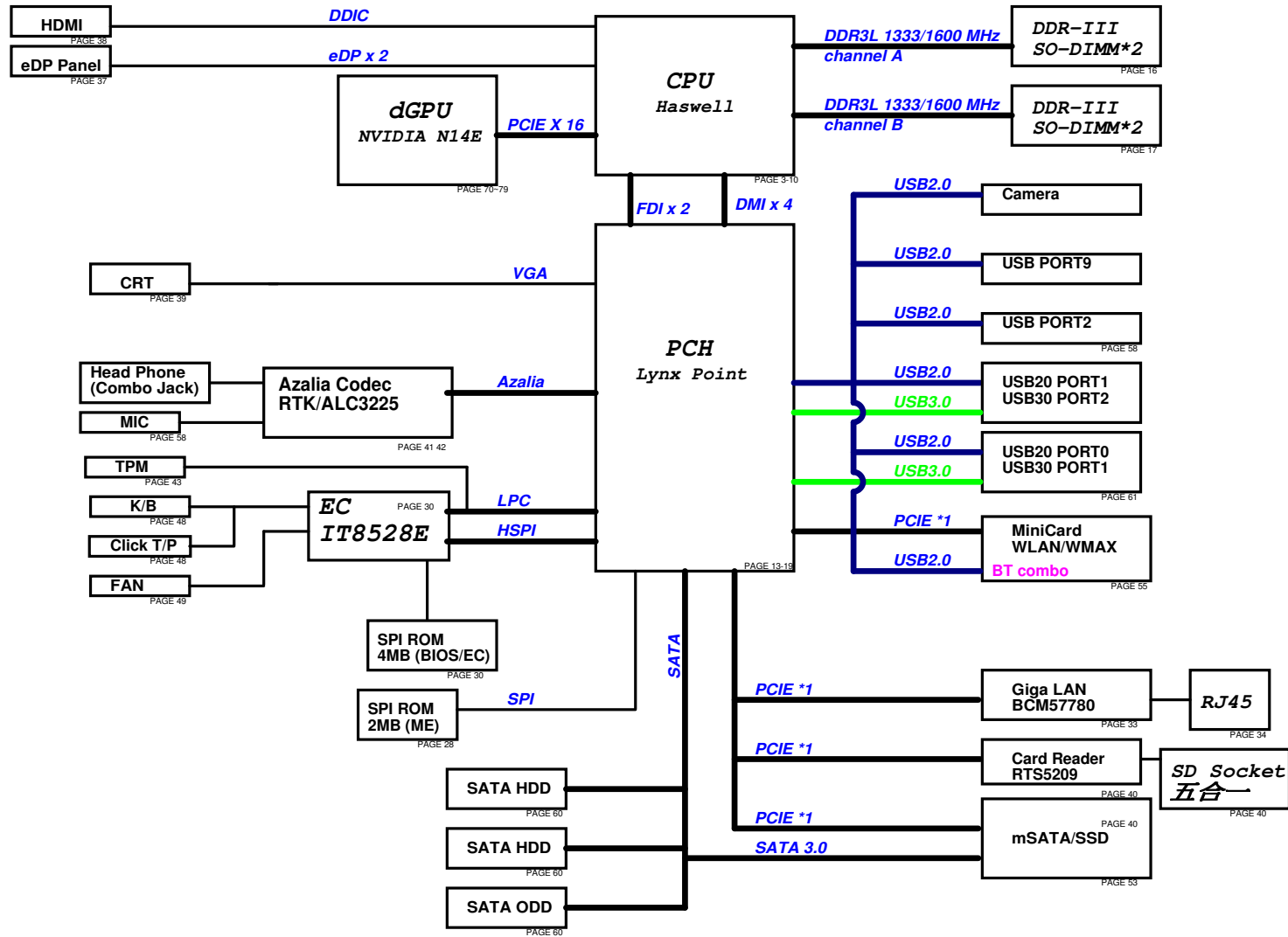


VA70HW BLOCK DIAGRAM



POWER

CPU VCORE	PAGE
SYSTEM, +3V, +5V	PAGE
+VCCP & +VCCP_V	PAGE
DDR & VTT	PAGE
2.5V & 1.5VS & 1.1V	PAGE
SMART CHARGER	PAGE
POWER DETECT	PAGE
LOAD SWITCH	PAGE
POWER PROTECT	PAGE

VGA POWER

GPU VCORE	PAGE 80
+1.05VS_VGA	
+3VS_VGA	
+12VS_VGA	
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

Power Rails

Sleep State	RTC	VA	VSUS	VS
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4	ON	ON	ON	OFF
S5/ AC	ON	ON	ON	OFF
S5/ DC	ON	ON	OFF	OFF

PCIe Port

PCIE_P1	CARDREADER
PCIE_P2	mSATA
PCIE_P3	Mini CARD (WLAN)
PCIE_P4	LAN
PCIE_P5	
PCIE_P6	

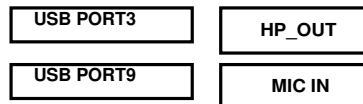
USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	External DB
USB P03	
USB P04	
USB P05	WiFi
USB P08	Camera
USB P09	External DB
USB F10	BT
USB F11	PCIe/mSATA
USB F12	
USB F13	

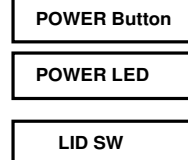
SATA PORT

SATA P0	HDD 1
SATA P1	
SATA P2	ODD
SATA P3	
SATA P4	mSATA
SATA P5	HDD 2

IO BOARD



PWR BOARD



R1.2 2012/11/26
reserved for 2014 processor

R1.2 2012/11/08
cost down 0ohm

R1.0 PU/PD for JTAG signals

R1.2 2012/11/27
design guide and check list use 1%
Intel CRB 1%

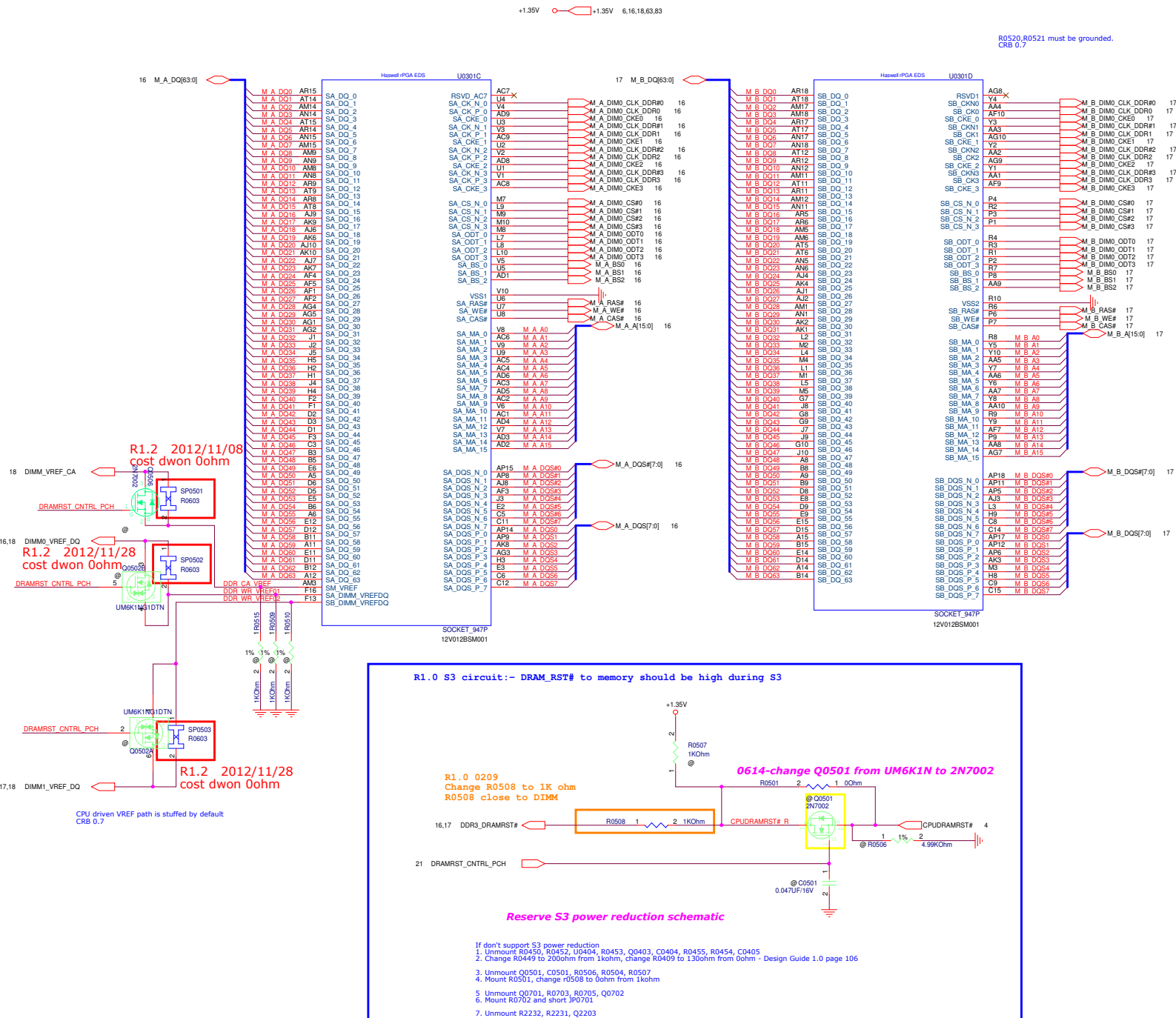
Intel MOW WW14:
change R0449, R0450 value

Power good for +1.35V_VCCDDQ (delay > 15ns)
Processor may be damaged if VIH exceeds the maximum voltage for extended periods.
SM_DRAMPWRK VIH MAX = 1.0V ; VIH MIN=0.45*VDDQ

+VCCIO_OUT 6.37,47.63
+1.35V_VCCDDQ 6
+3VSUS 22.23,27.28,30.33,43.61,81.92
+3V 37.43,63.65,91
+1.05VS 25.26,27.47,63.80,82
+VCCIOA_OUT 3.6

R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R0436~R0439 for GDDR5

R1.2 2012/10/29
option changed from /FDI



VDDQ 22uF * 11 pcs (stuff)
10uF * 10 pcs (stuff)
330uF * 2 pcs (stuff)

VDDQ 22uF * 2pcs (stuff)
10uF * 2pcs (stuff)
330uF * 1pcs (stuff)

```
+VCORE 10uF * 11pcs (stuff)
        22uF * 19pcs (stuff)
        470uF * 4pcs (stuff)
```

```
+VCORE 10uF * 11 pcs (stuff)
        22uF * 19 pcs (stuff)
        470uF * 5 pcs (stuff)
```

Default: no support
S3 power reduction

Placement note:

1. R0602 close to CPU
2. R0603 close to CPU
3. R0605 close to VR
4. R0608 close to CPU
5. R0607 close to VR
6. R0611 close to CPU

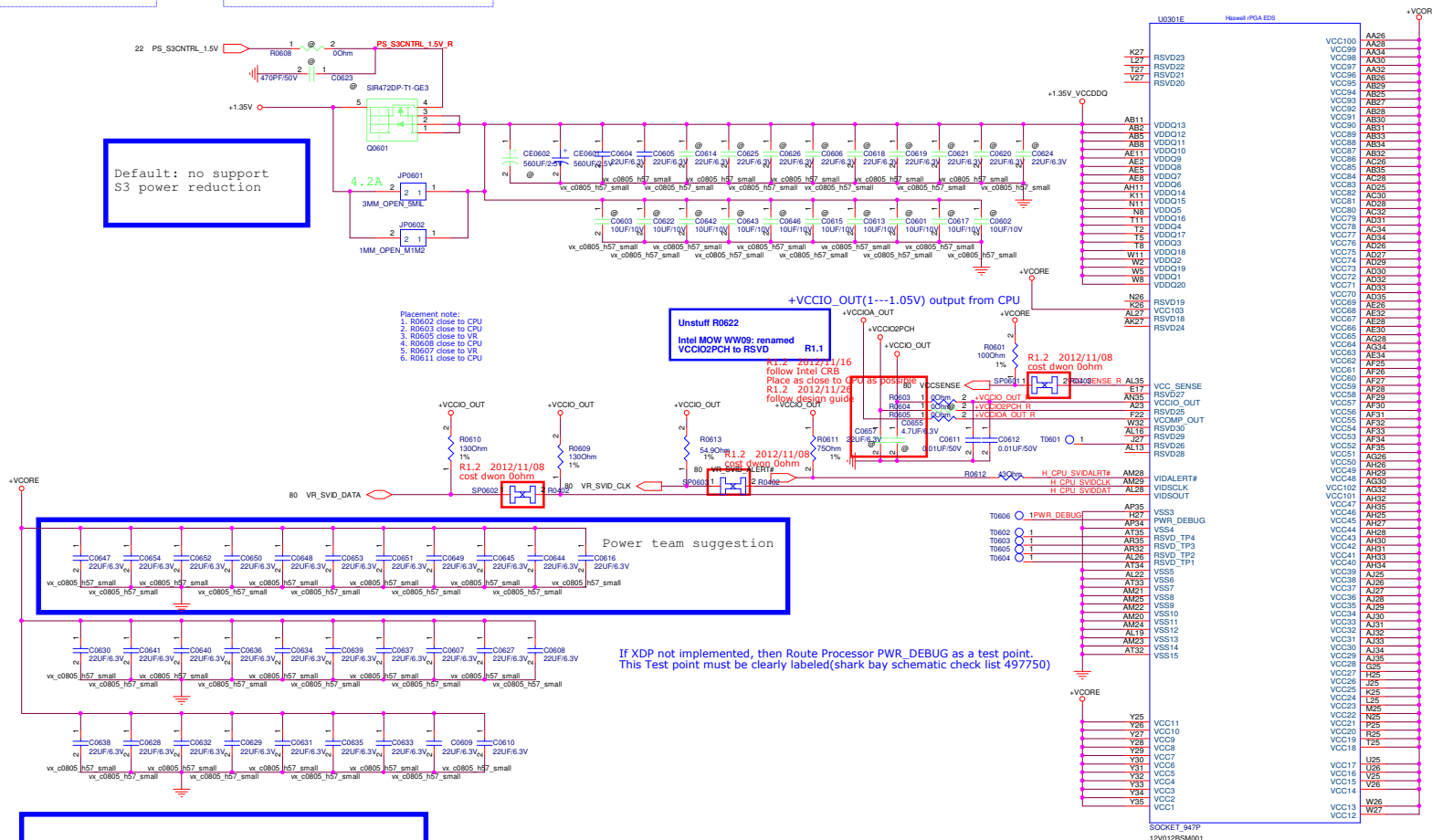
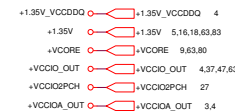
Unstuff R0622
Intel MOW WW09

[illegible]

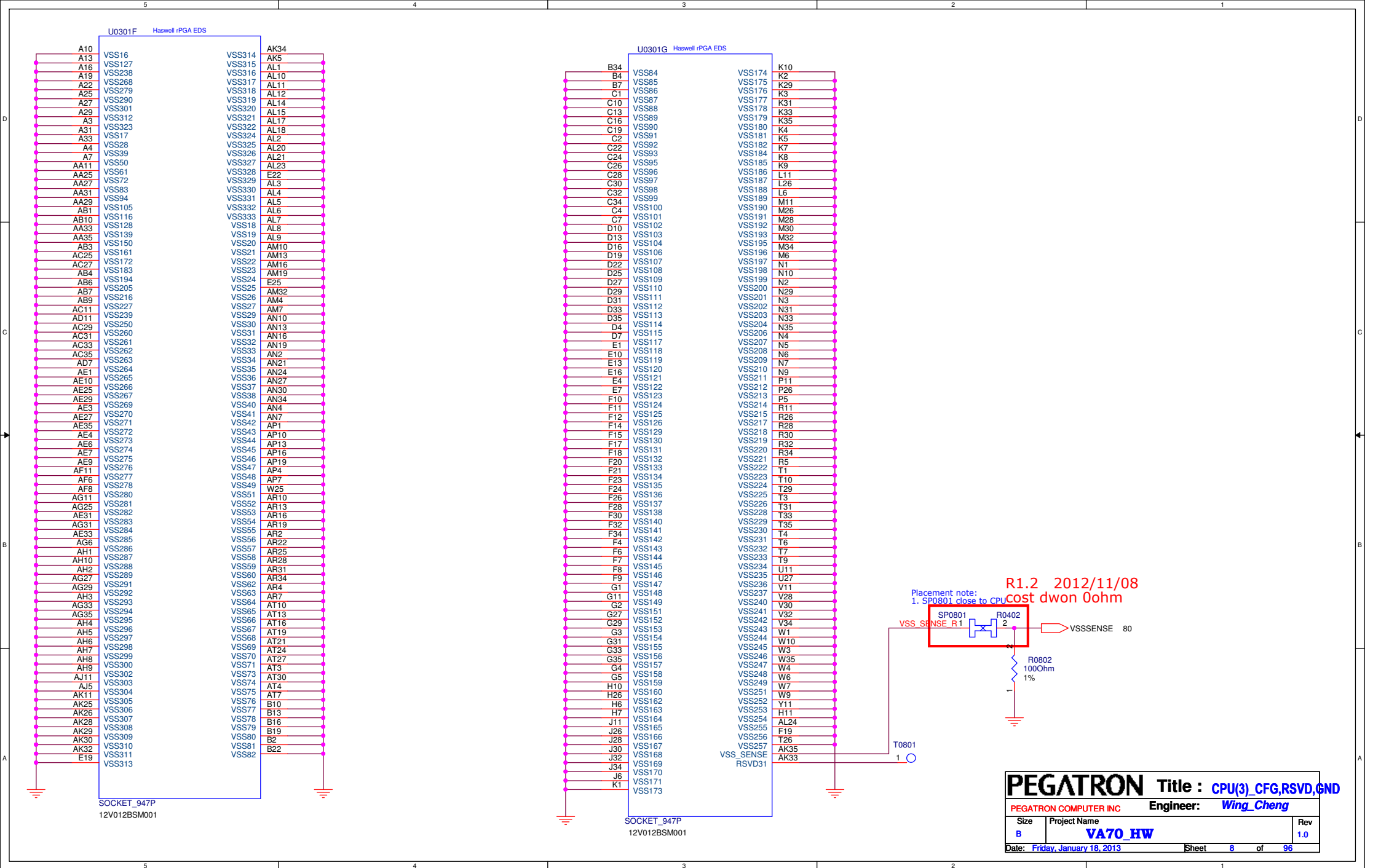
Power team suggestion

If XDP not implemented, then Route Processor PWR_DEBUG as a test point.
This Test point must be clearly labeled(shark bay schematic check list 497750)

Cap of 470UF or more place at power schematic







CFG strapping information: The CFG signals have a default value of '1'

CFG[1:0]: Reserved configuration lane.

CFG[2]: PCIe Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

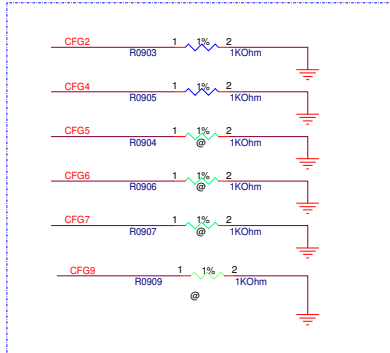
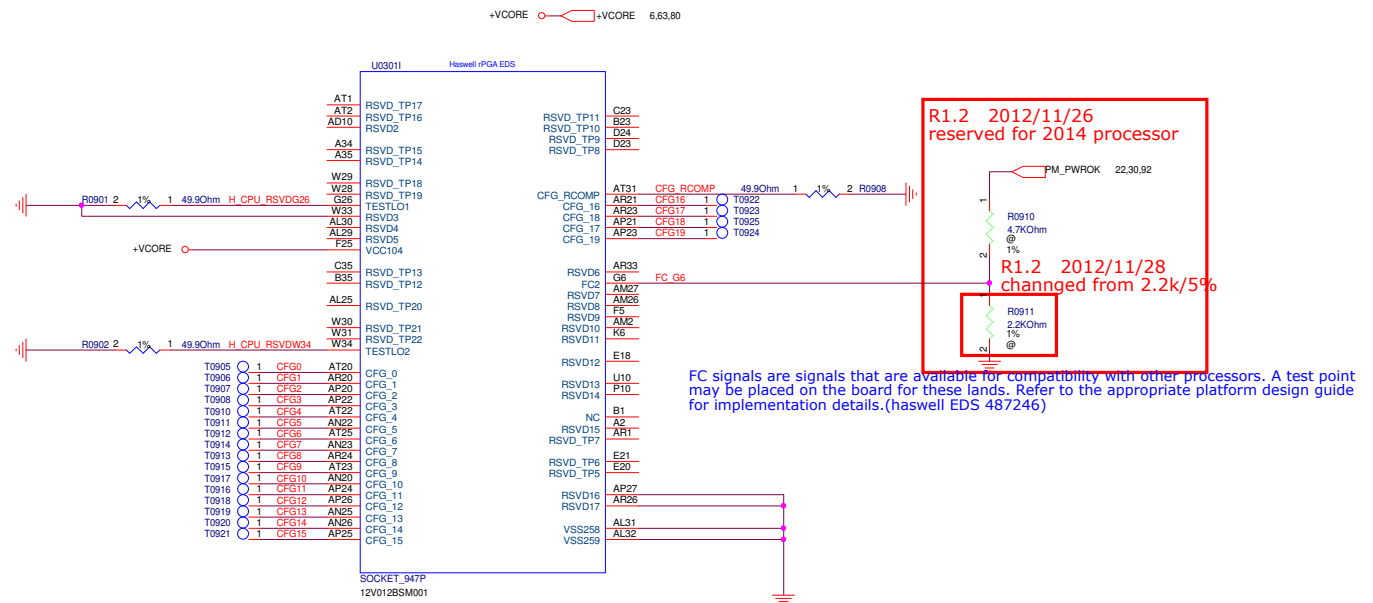
CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[6:5]: PCI Express Port Bifurcation Straps

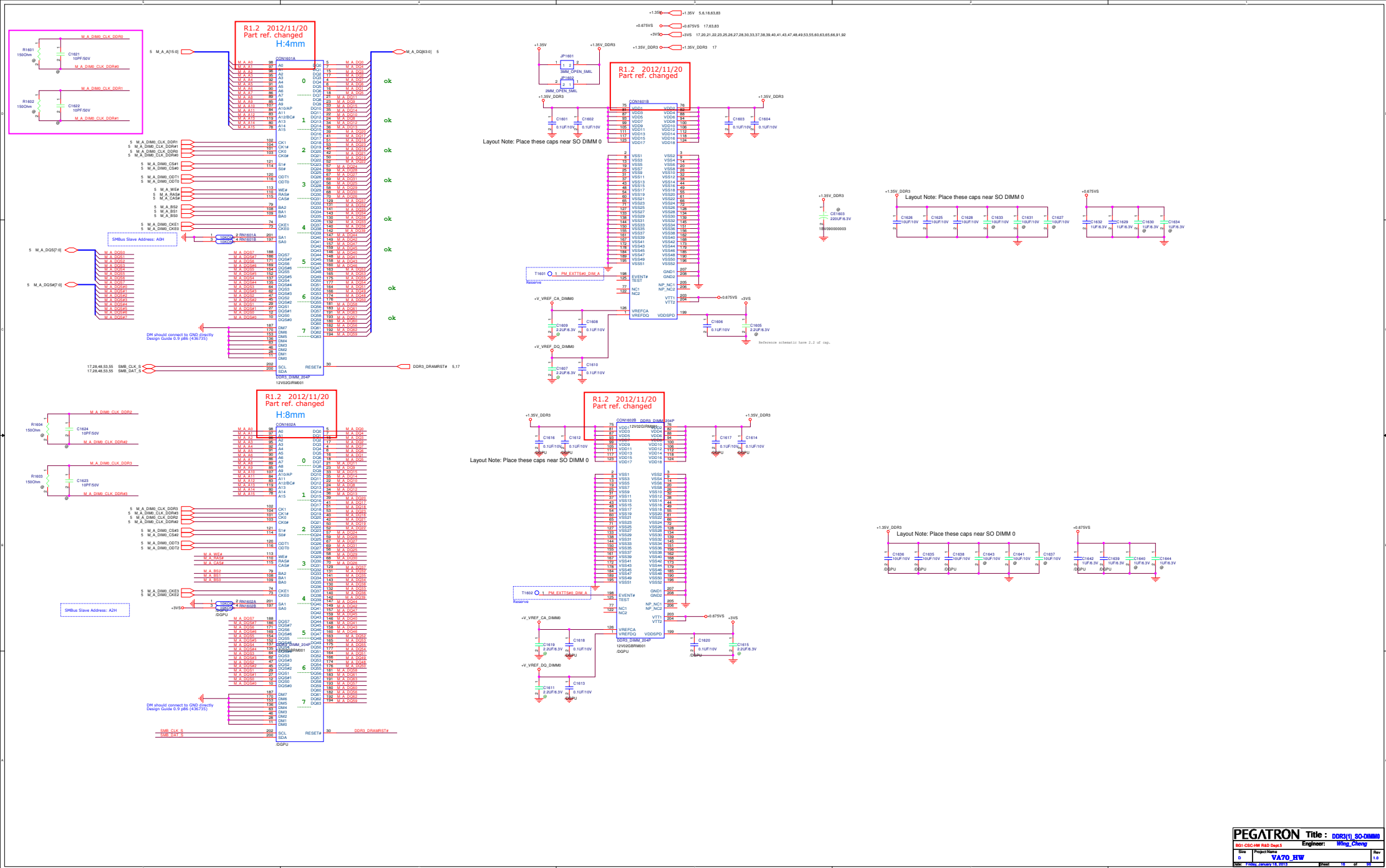
-00 = 1 x8, 2 x4 PCI Express*
-01 = reserved
-10 = 2 x8 PCI Express*
-11 = 1 x16 PCI Express*

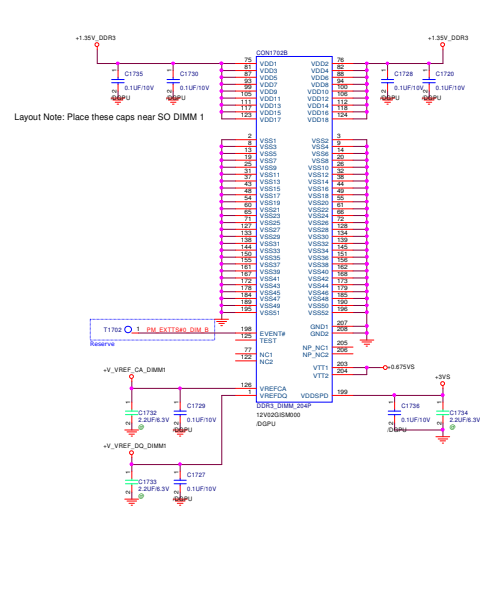
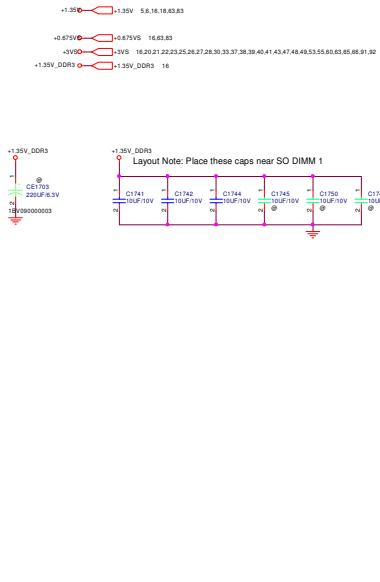
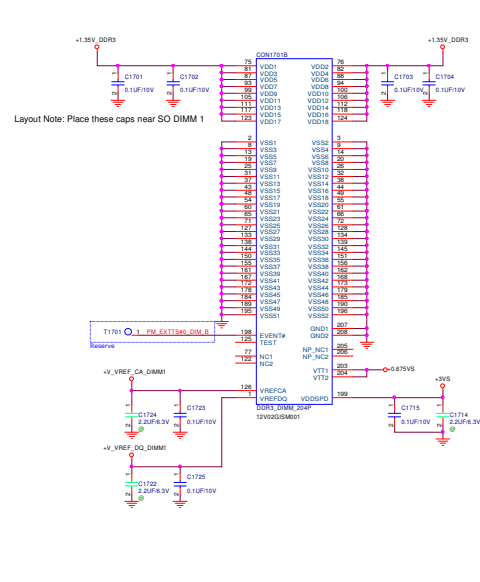
CFG[19:7]: Reserved configuration lane.



PEGATRON		Title : CPU(3)_CFG,RSVD,GND	
PEGATRON COMPUTER INC		Engineer: Wing_Cheng	
Size	Project Name	Rev	
Custom	VA70_HW	1.0	
Date: Friday, January 18, 2013		Sheet	9 of 96

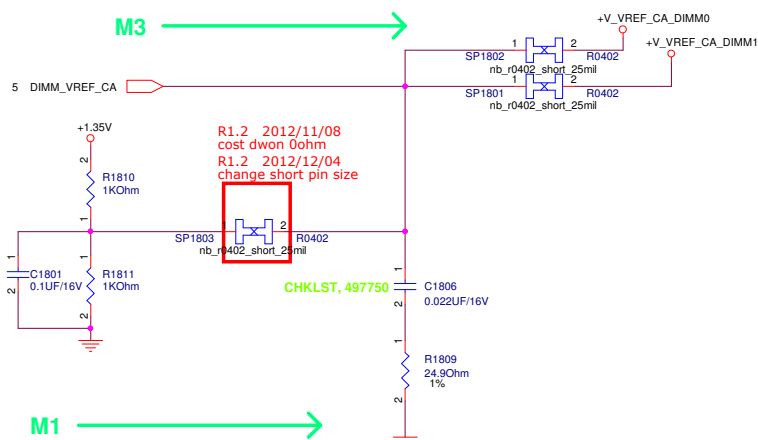
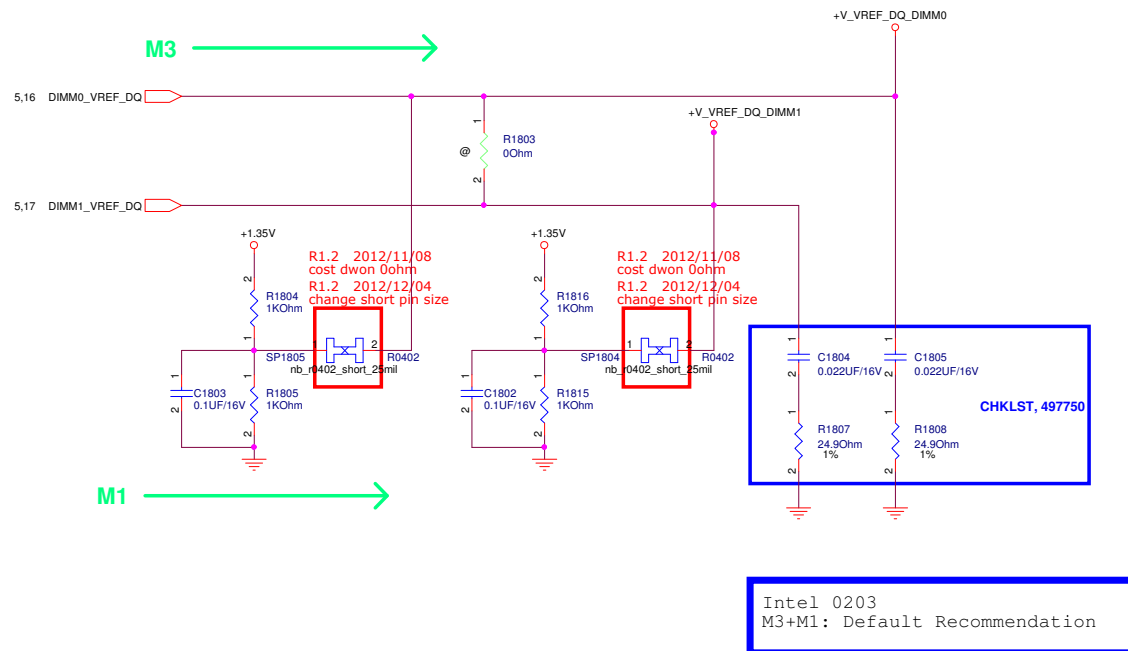
PEGATRON		Title : NB(3)_****	
PEGATRON COMPUTER INC		Engineer: <i>Wing_Cheng</i>	
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013	Sheet	10	of 96



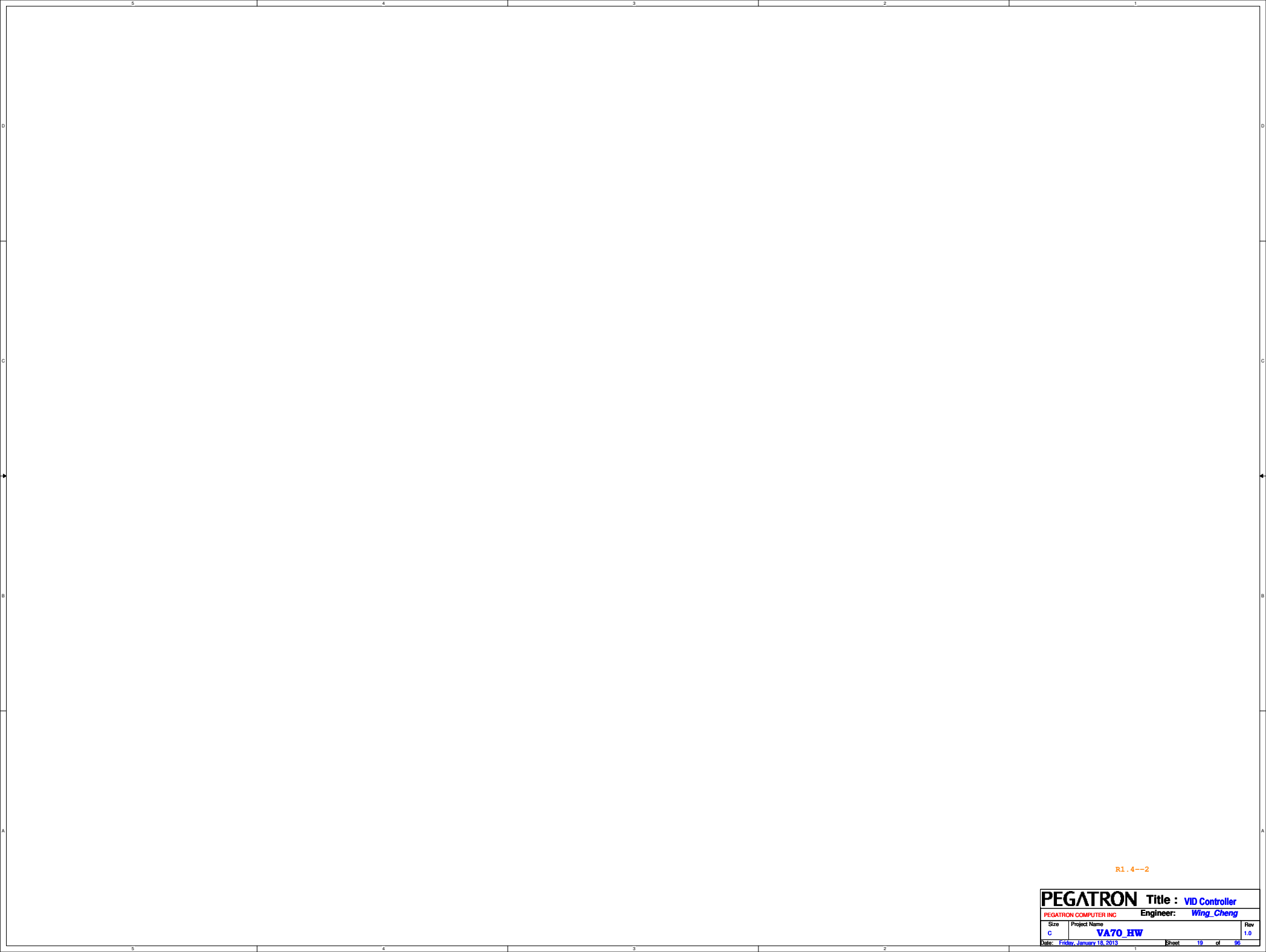


DDR3L Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

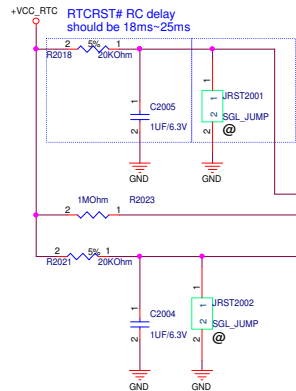
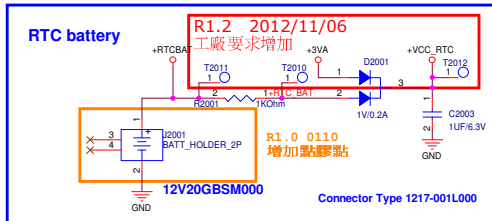


+1.35V_DDR3 16,17
+V_VREF_CA_DIMM0 16
+V_VREF_DQ_DIMM0 5,16
+V_VREF_CA_DIMM1 17
+V_VREF_DQ_DIMM1 5,17

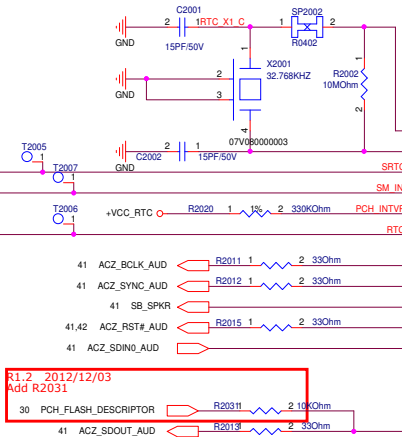


R1.4--2

PEGATRON		Title : VID Controller	
PEGATRON COMPUTER INC		Engineer: Wing Cheng	
Size	Project Name		Rev
C	VA70 HW		1.0
Date: Friday, January 18, 2013		Sheet	19 of 95

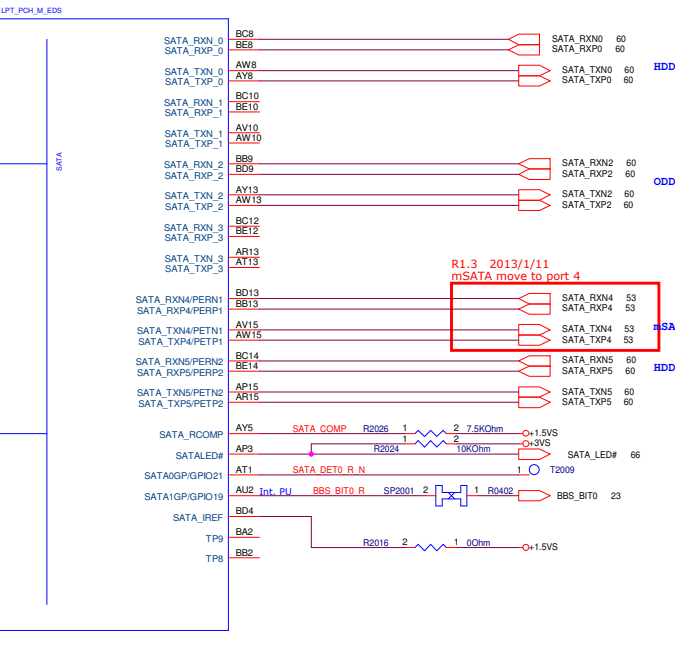
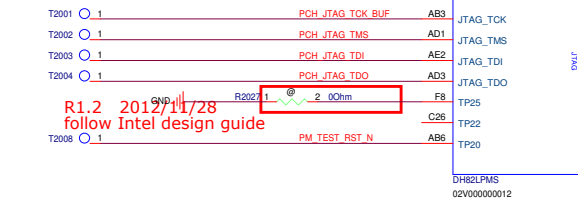
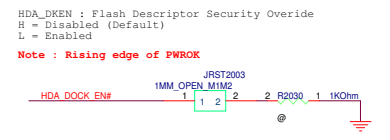
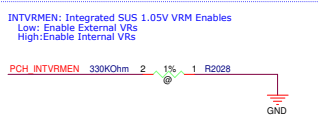


TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

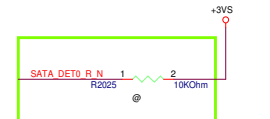
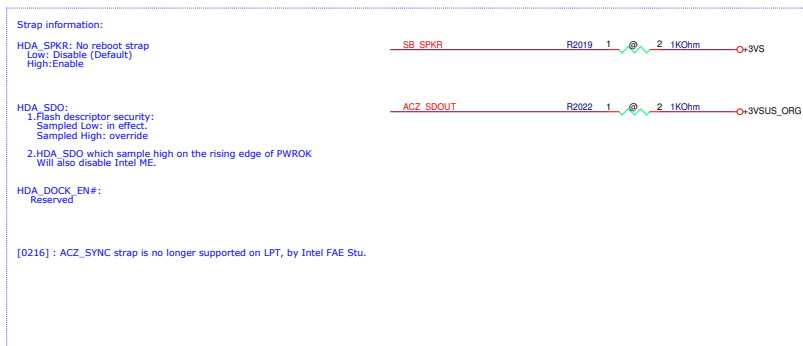


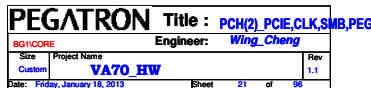
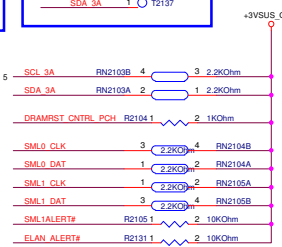
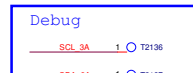
Request by CSC for CMOS clear function

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)



SATA0GP's pull up 電阻 (參考線路(43K ohm)和check list(10K ohm))寫的不同??先照參考線路





R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/12/06
remove R2335~R2337, R2339~R2341, JP2304~JP2306 for GDDR5

R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA
R1.3 2013/1/8
R2332~R2334 are removed

R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA

R1.2 2012/11/27
follow intel design guide remove R2348 for GDDR5
co-lay with R2332
R1.2 2012/12/19
option changed from /non_RETINA

R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R2338, R2329~R2331, R2349 for GDDR5

R1.2 2012/11/27
follow intel design guide

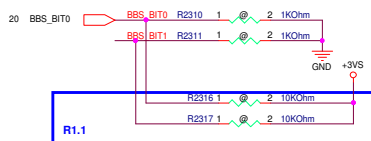
CRT Disable: (For discrete graphic)

1. NC:
CRT_R,CRT_G,CRT_B
CRT_HSYCN,CRT_VSYN
2. 1KΩ+-5% pull-down to GND:
3. Connected to GND:
CRT_ITRN
DAC_IREF
4. Connect to +V3.3:
VCCADAC

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI (PCH) DEFAULT

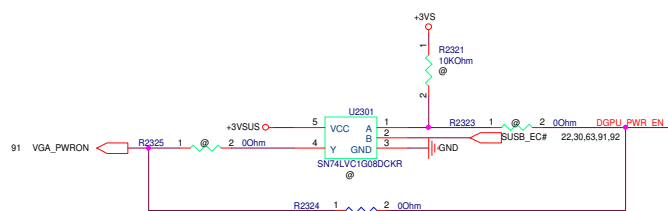
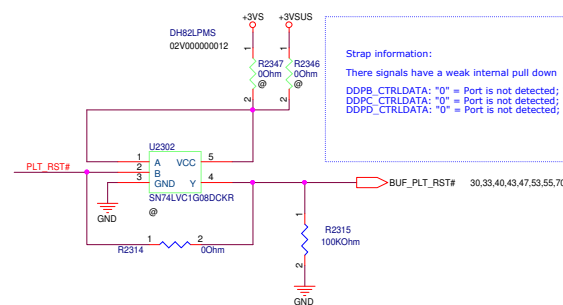
Sampled on rising edge of PWROK.



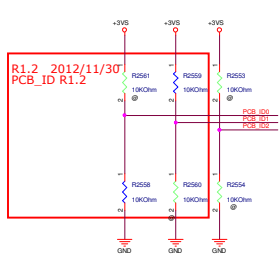
STP_A16OVR: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/
Top-Block swap override

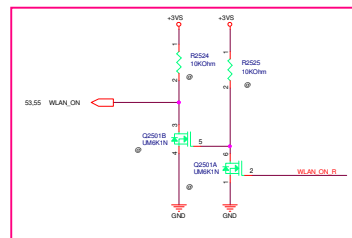
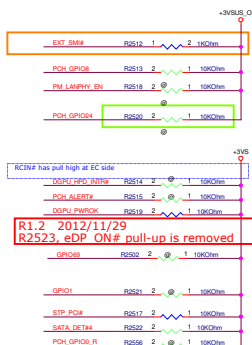
High=Default



+3VS 16,17,20,21,22,25,26,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3V 37,43,63,65,91

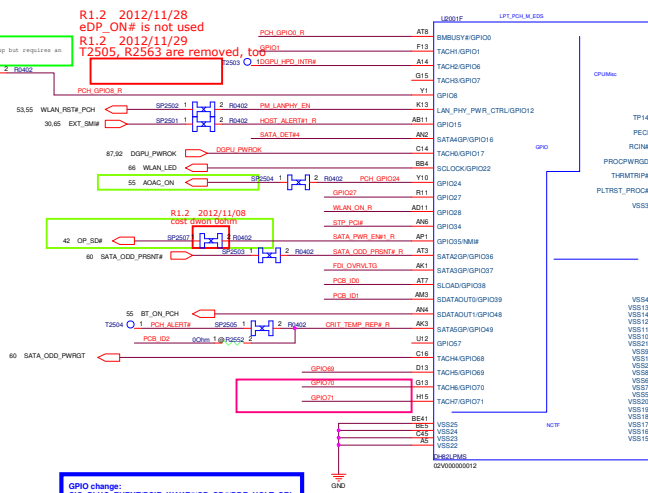


PCB_ID	PCB_ID1	PCB_ID0
R1.0	TBD	0
R1.1	TBD	0
R1.2	TBD	1
R1.3	TBD	1



Functional Signal Definitions:
 (Logic: RLS Confidentiality (Intel Crypto Transport Layer Security))
 "1" = Enable
 "0" = Disable
 1. This internal pull-down is disabled after PLTRSTF deasserts.
 2. This signal should not be pulled high when strap is sampled.

R1.2 2012/11/28
 eDP_ON# is not used
 R1.2 2012/11/29
 T2505, R2553 are removed, too



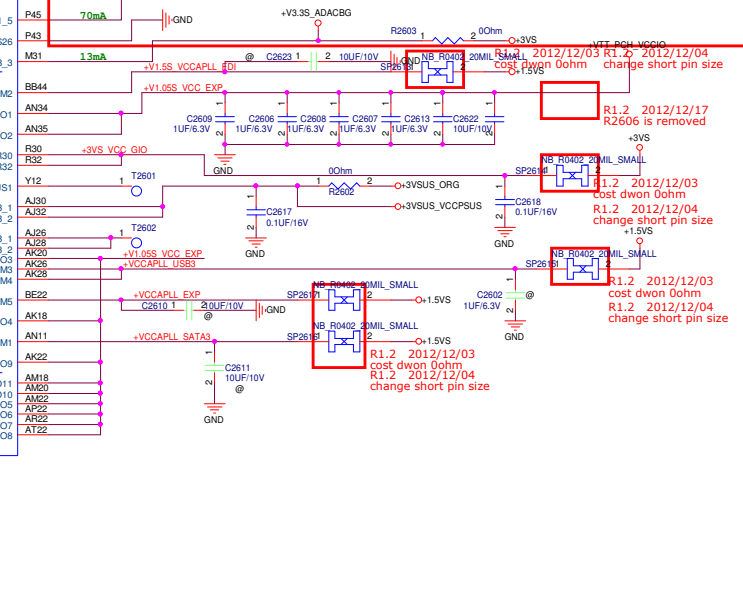
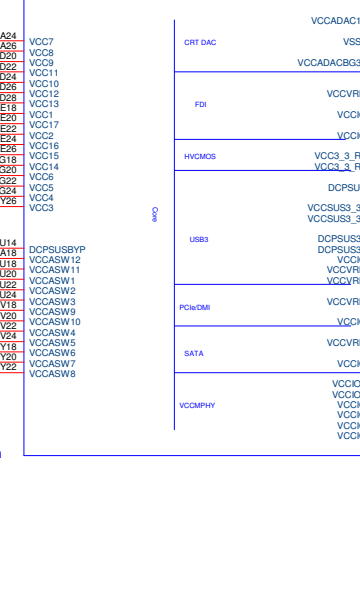
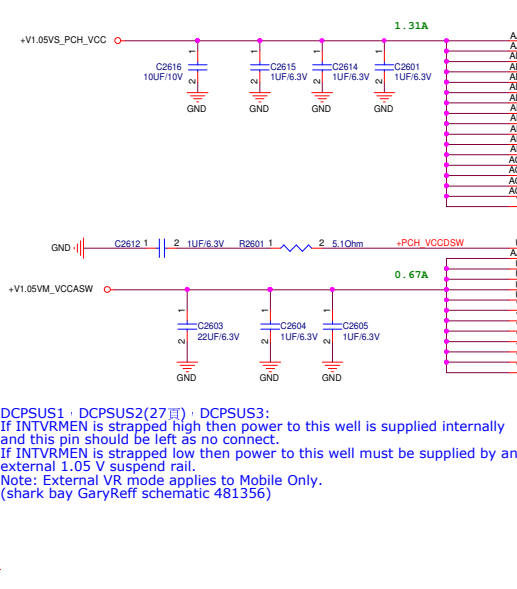
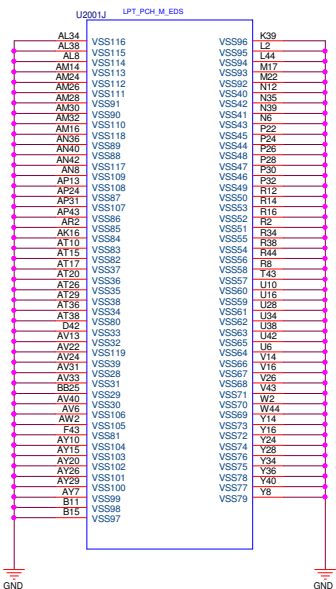
GPIO change:
 GPIO_PLUG_EVENT/PCIE_WAKE/OP_SD#DDR_VOLT_SEL
 PCB_ID#



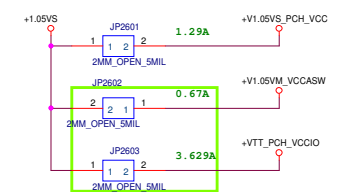
USB3 Port 3 PCIE Port2 Mode (USB3P3_PCIEP2 MODE)
 USB3p3 each6_gp70 pin is a '0', then Root Port 2 is assigned to USB3 Port 3, else it is assigned to PCI Express.
 USB3 Port 2 PCIE Port1 Mode (USB3P2_PCIEP1 MODE)
 USB3p3 each7_gp71 pin is a '0', then Root Port 1 is assigned to USB3 Port 2, else it is assigned to PCI Express.

TP14 is Intel Reserved Pin: Must have a pull up resistor to VCC3_3. Standard resistor value in the range of 4.7K to 15K ok(shark bay LPT EDS 486708)

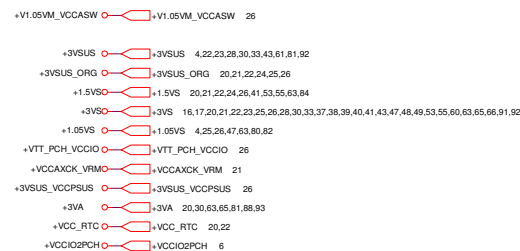
need close to EC

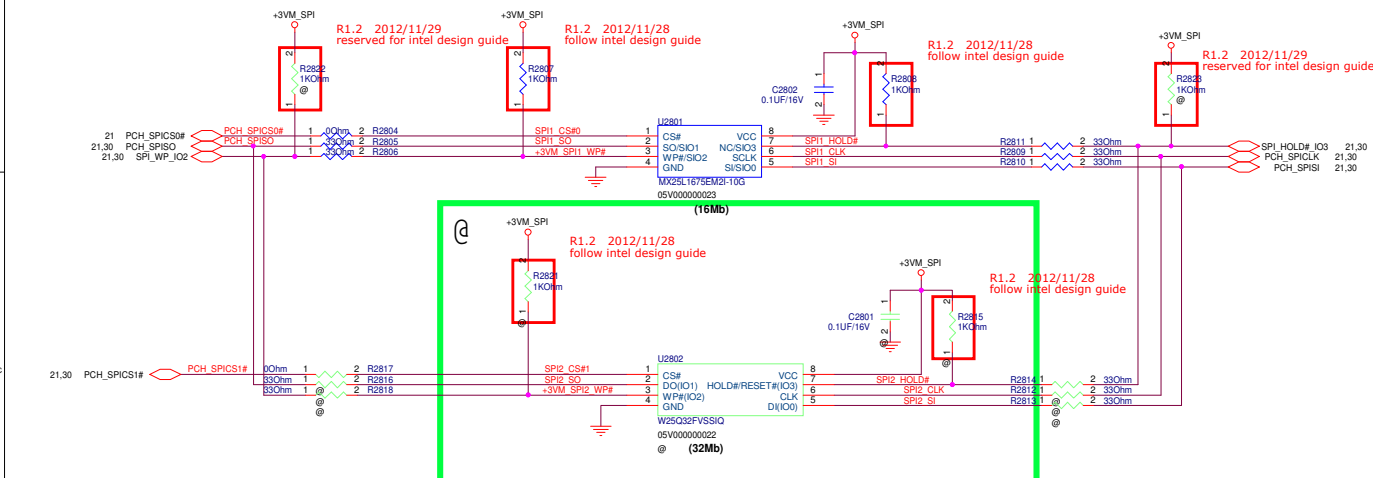












DCPSUS1 : DCPSUS2(27) : DCPSUS3:
If INTVRMEN is strapped high then power to this well is supplied internally
and this pin should be left as no connect.
If INTVRMEN is strapped low then power to this well must be supplied by an
external 1.05 V suspend rail.
Note: External VR mode applies to Mobile Only.
(shark bay GaryReff schematic 481356)

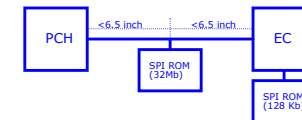


- +V1.05VS_VCCASW → +V1.05VS_VCCASW 27
- +VTT_PCH_VCCIO → +VTT_PCH_VCCIO 27
- +1.05VS → +1.05VS 4,25,27,47,63,80,82
- +1.5VS → +1.5VS 20,21,22,24,27,41,53,55,63,84
- +3VS → +3VS 16,17,20,21,22,23,25,27,28,30,33,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
- +3VSUS_VCCPSUS → +3VSUS_VCCPSUS 27





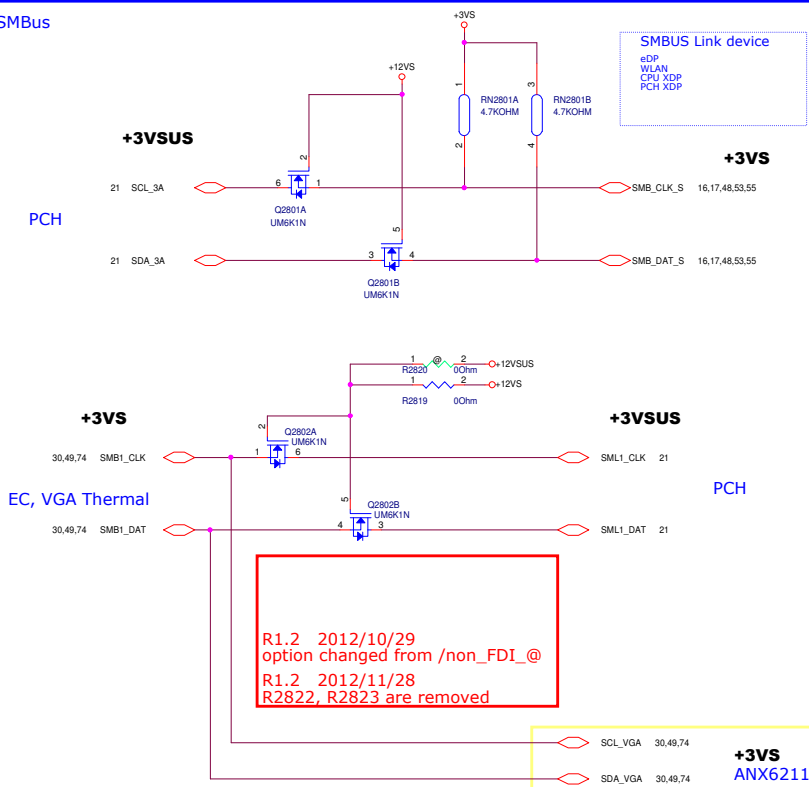
+3VSUS			+3VS	16, 17, 20, 21, 22, 23, 25, 26, 27, 30, 33, 37, 38, 39, 40, 41, 43, 47, 48, 49, 53, 55, 60, 63, 65, 66, 91, 92
+12VS			+12VS	39, 41, 63, 91
+12VSUS			+12VSUS	22, 33, 55, 60, 81, 91
+3VM_SPI			+3VM_SPI	27
+3VSUS			+3VSUS	4, 22, 23, 27, 30, 33, 43, 61, 81, 92



ROM setting:
Configuration 1. ITE HSPI -> short J2803 pin2 & 3
and no stuff U2801,U2802
Configuration 2. One ROM location -> short J2803 pin1&2
and no stuff U2802 ; stuff U2801(BIOS+ME)
Configuration 3. Two ROM location -> short J2803 pin1&2 , J2802 pin2&3
Stuff U2801 (ME), Stuff U2802 (BIOS)

```
Follow Intel setting:
U2801: ME
U2802: BIOS
```

PCH SMBus



R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/11/28
R2822, R2823 are removed

PEGATRON		Title :	PCH(9)_SPI,SMB
PEGATRON COMPUTER INC		Engineer:	Wing_Cheng
Size C	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013		Sheet	28 of 96

	5	4	3	2	1
D					
C					
B					
A					

PEGATRON		Title : CLK_JCS9LRS3197	
PEGATRON COMPUTER INC		Engineer: Wing_Cheng	
Size Custom	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013		Sheet 29 of 96	

+3VA_EC 38.47
+3V5 18.17,20.21,22.23,25.26,27.28,30,37,38,39,40,41,43,47,48,49,53,55,60,63,65,66,91,92
+3V5B 4.22,23,27,28,30,43,61,81,92
+3VA 20.27,63,65,81,92,93



R1.2 2012/11/08
cost down 0ohm

R1.2 2012/11/06
工廠要求增加

R1.2 2012/11/06
工廠要求增加

R1.2 2012/11/08
cost down 0ohm
R1.2 2012/11/28
change back to 0ohm
R1.2 2012/11/06
R3042, R3044 are replaced by SP3008, SP3012
R1.2 2012/11/17
SP3008, SP3012 replaced by 0ohm

R1.2 2012/11/08
cost down 0ohm
R1.2 2012/11/28
change to 33ohm for Intel check list
R1.2 2012/12/07
R3056~R3059 are replaced by SP3014, SP3015, SP3019, SP3020
R1.2 2012/12/17
SP3014, SP3015, SP3019, SP3020 are replaced by 0ohm

Cloud=12.SPF
place close to EC

non-Share ROM

Share ROM

need to check ROM P/N

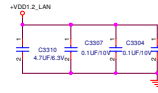
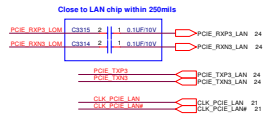
For PU / PD

R1.2 2012/11/08
follow MA50

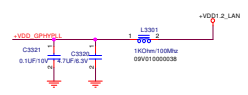
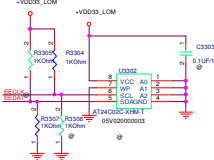
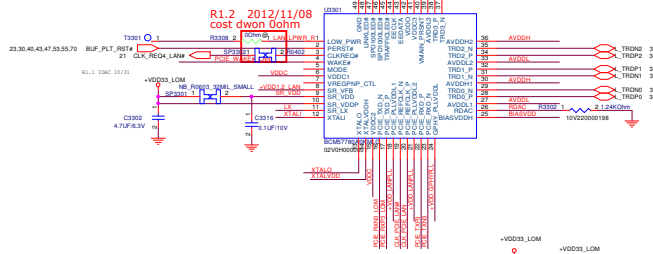
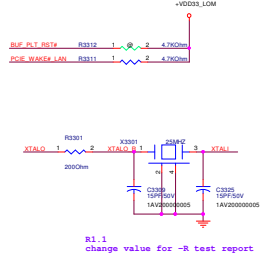
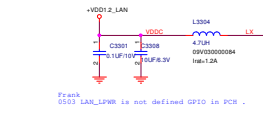
R1.2 2012/12/05
R3065 changed to 0

R1.2 2012/11/30
cost down

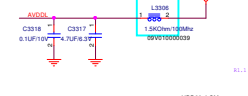
PEGATRON Title : ITERS28E			
REV:001	Project Name	Engineer	Wing Cheng
Drawn	VA70 HW	Check	1.0
Date: Friday, January 18, 2013		Drawn	30 of 80



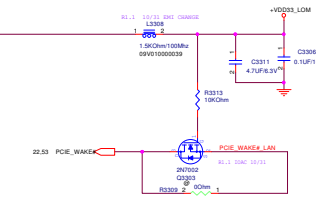
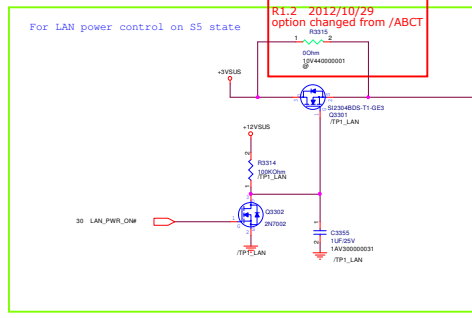
R1.2 2012/10/29
pin 46-48 has been connected together.



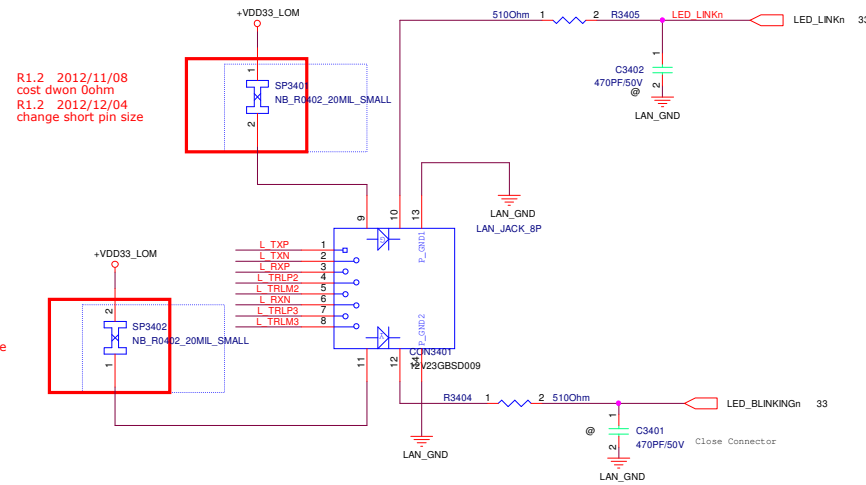
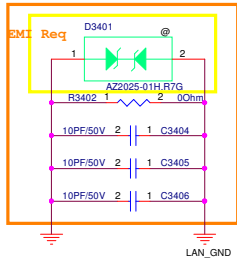
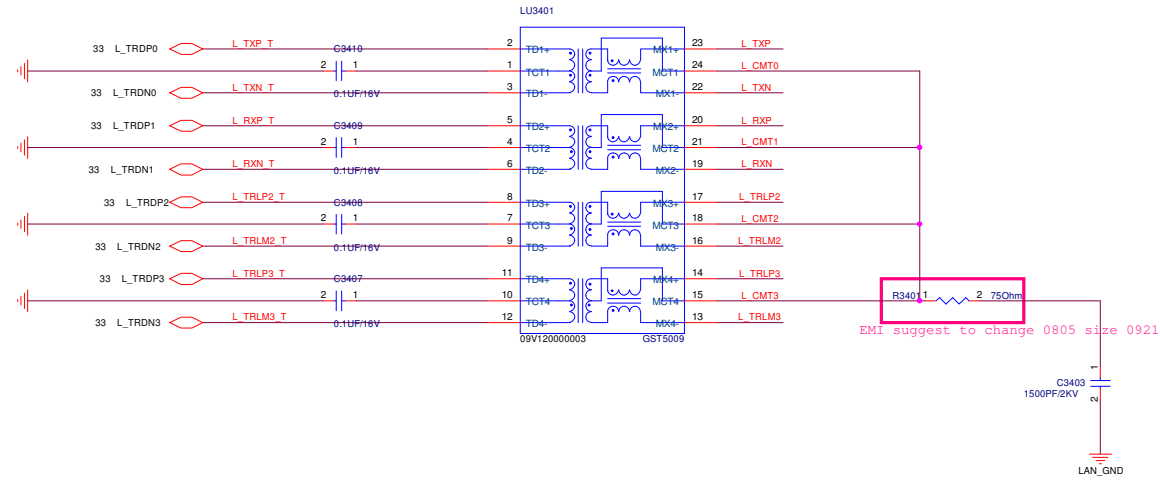
R1.2-26 EMI



PEGATRON Title : LAN RTL8111			
B01-18W RD Ch2-18W RD Dap1.3		Engineer: Wing Cheng	
Rev	Project Name	Rev	Rev
0	VA70 HW	0	0
Rev	Rev	Rev	Rev
0	0	0	0



Co-Layout



<Variant Name>

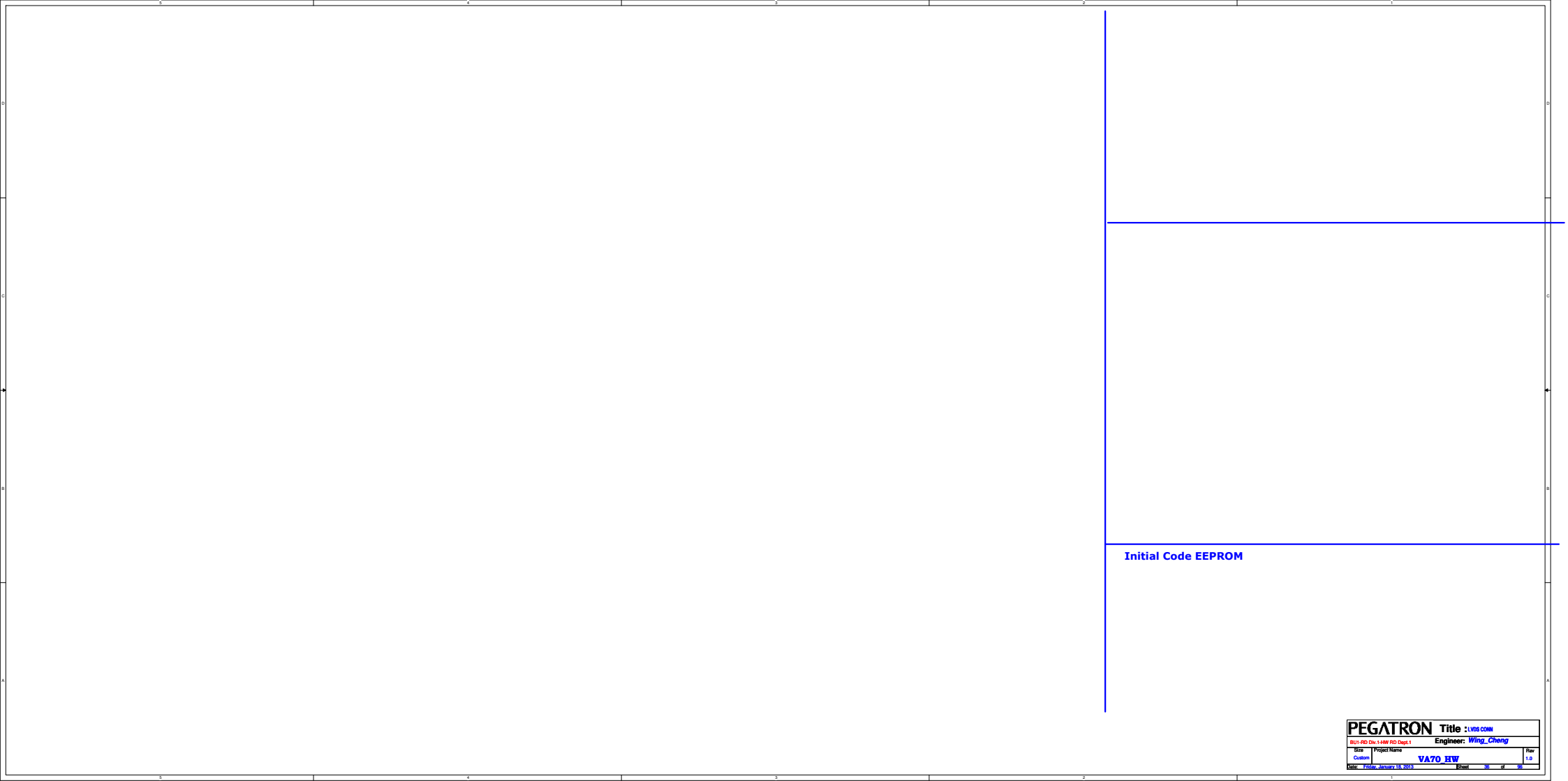
PEGATRON Title : RJ45 RJ11

BG1 CSC-HW R&D Dept.5 Engineer: Wing Cheng

Size	Project Name	Rev
Custom	VA70_HW	1.0

Date: Friday, January 18, 2013 Sheet 34 of 95

The image shows a large, empty rectangular area, likely a drawing or image, framed by a thick black border. The area is mostly white, with some faint, illegible text visible in the bottom right corner, likely a title block or metadata. The text in the bottom right corner includes "Pegatron", "Title: SP to VGA", "Rev: 1.0", and "Date: Friday, January 18, 2013".



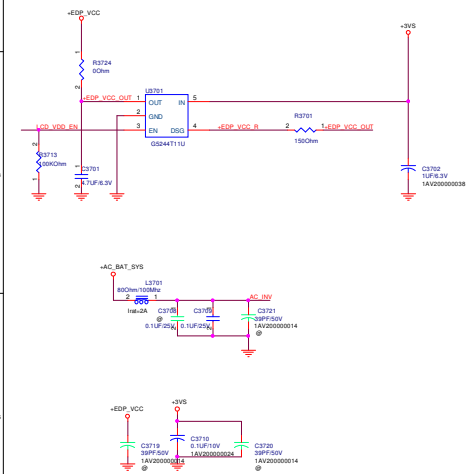
PEGATRON		Title: 2 LVDS CONN	
S11-RD Dns 1.44M RD Dns 1.7		Engineer: <u>Wing_Cheng</u>	
Size	Project Name		Rev
Custom	VA70 HW		1.0
Date: Friday, January 18, 2019		Sheet	36 of 36

LVDS

CH A

CH B

eDP



From CPU

EXP_AUXP	C3716	1	2	EXP_AUXP
EXP_AUXN	C3717	1	2	EXP_AUXN
EXP_TAP0	C3722	1	2	EXP_TAP0
EXP_TAPN	C3718	1	2	EXP_TAPN
EXP_TAP1	C3724	1	2	EXP_TAP1
EXP_TAPN	C3723	1	2	EXP_TAPN

R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove C3727~C3730 for GDDR5

H

HPD low active

From CPU

HPD

R1.2 2012/11/15
Changing to 30pins+10pins

R1.2 2012/11/19
Pin mapping changed

R1.2 2012/11/29
P/N changed to 32V37GBSM011
R1.2 2012/11/29
option changed from N/A
~~R1.2 2012/12/06
remove CON3704 for GDDR5~~

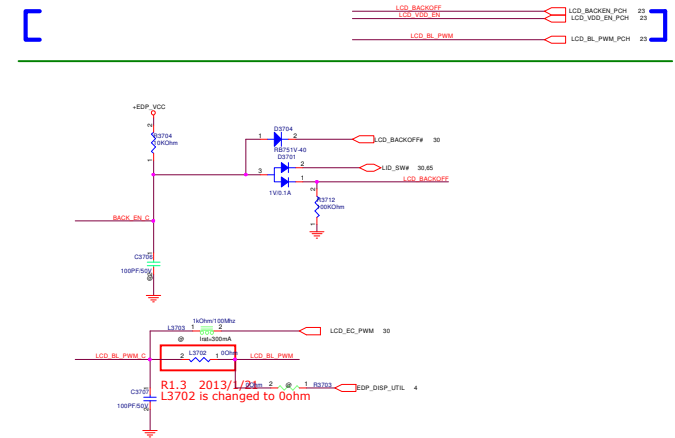
R1.2 2012/11/26
prevent +EDP_VCC voltage drop
R1.2 2012/11/28
SCL, SDA changed to +EDP_VCC
R1.2 2012/11/28

R1.2 2012/
P/N changed

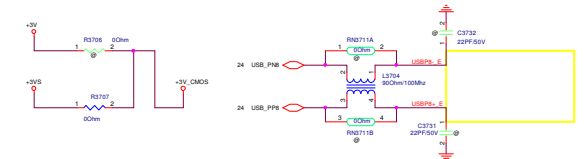
LVDS/eDP control signal

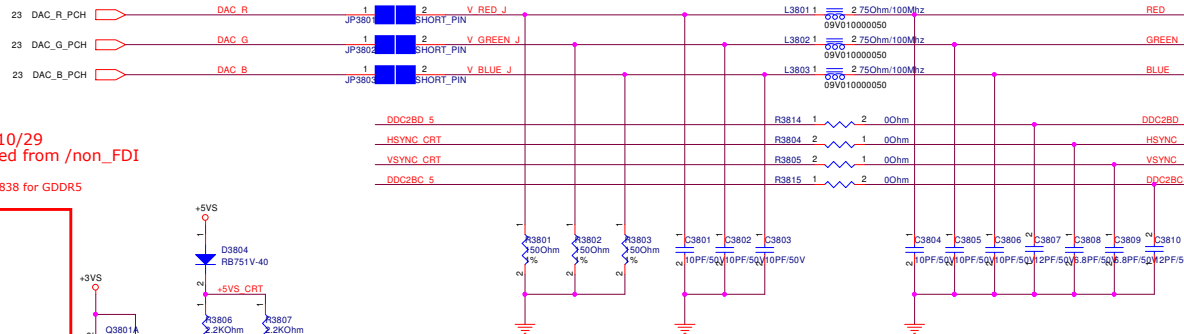
LVDS/EDP共用pin

LVDS/EDP共用pin



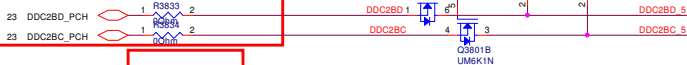
USB Camera



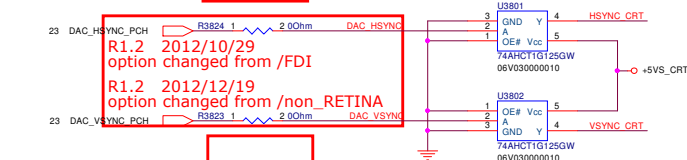


R1.2 2012/10/29
option changed from /non_FDI
R1.2 2012/12/06
remove R3837, R3838 for GDDR5

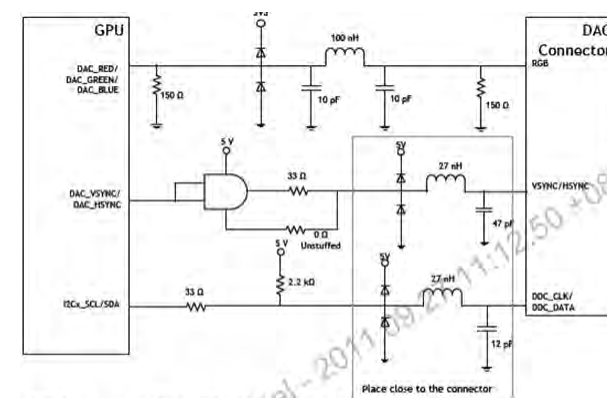
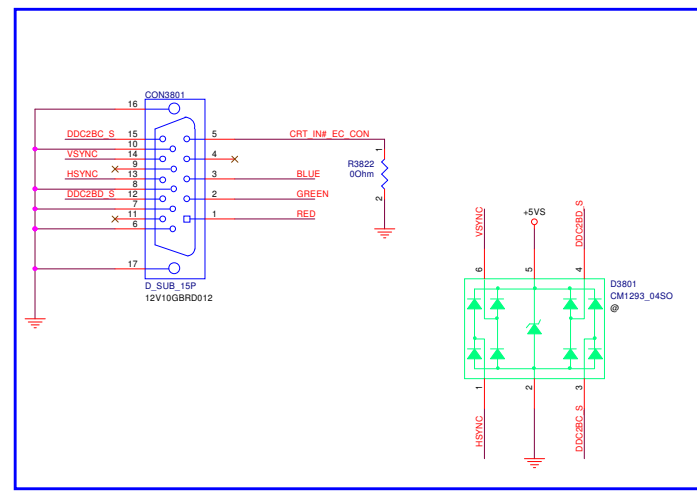
R1.2 2012/10/29
option changed from /FDI
R1.2 2012/12/19
option changed from /non_RETINA



R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/12/06
remove R3825, R3826, R3835, R3836 for GDDR5



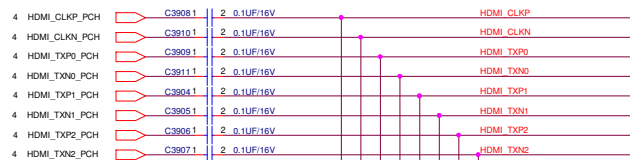
R1.2 2012/10/29
option changed from /non_FDI_@
R1.2 2012/12/06
remove R3825, R3826, R3835, R3836 for GDDR5



RSET Requirements: DACA_RSET= 124 Ω, 1%, stuffed by default.

Figure 71. GPU-DAC Connections

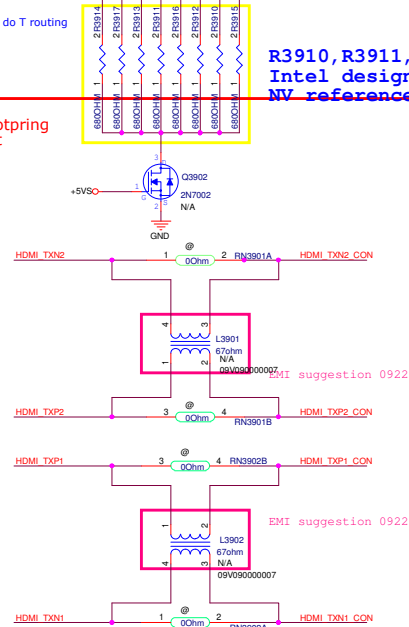
The LC filter circuit (NV DSC only)
DDC: L=27nH, C=12PF
HSYNC/VSYNC: L=27nH, C=47PF
RGB: L=100nH, C=10PF



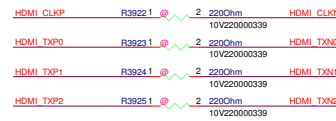
Close to connector and do T routing

R3910, R3911, R3912, R3913, R3914, R3915, R3916, R3917
Intel design guide : 680ohm /UMA
NV reference schematics : 499ohm /DGPUO

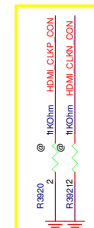
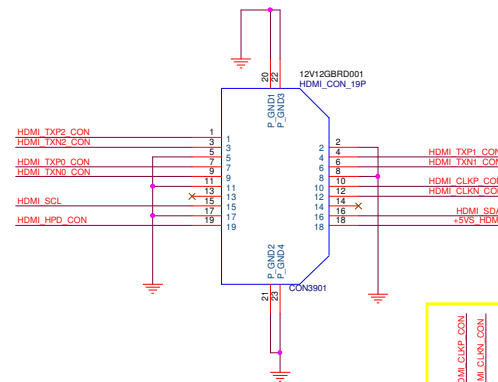
R1.2 2012/12/03
L3901~L3904 are changed to 90ohm for layout to change footprint
0ohm are removed cause they can't co-lay with new footprint
R1.2 2012/12/04
L3903, L3902 pin mapping changed
Add RN3901~RN3904 for layout
R1.2 2012/12/11
changed to 45ohm
R1.3 2013/1/15
changed to 67ohm
R1.3 2013/1/16
L3901~L3904 are swapped



EMI solution



HDMI_SCL & HDMI_SDA : no via , trace length should be as short as possible

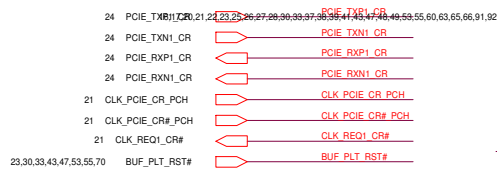


EMI solution

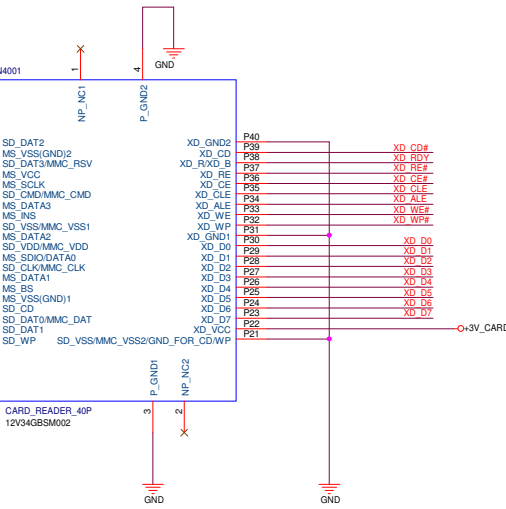
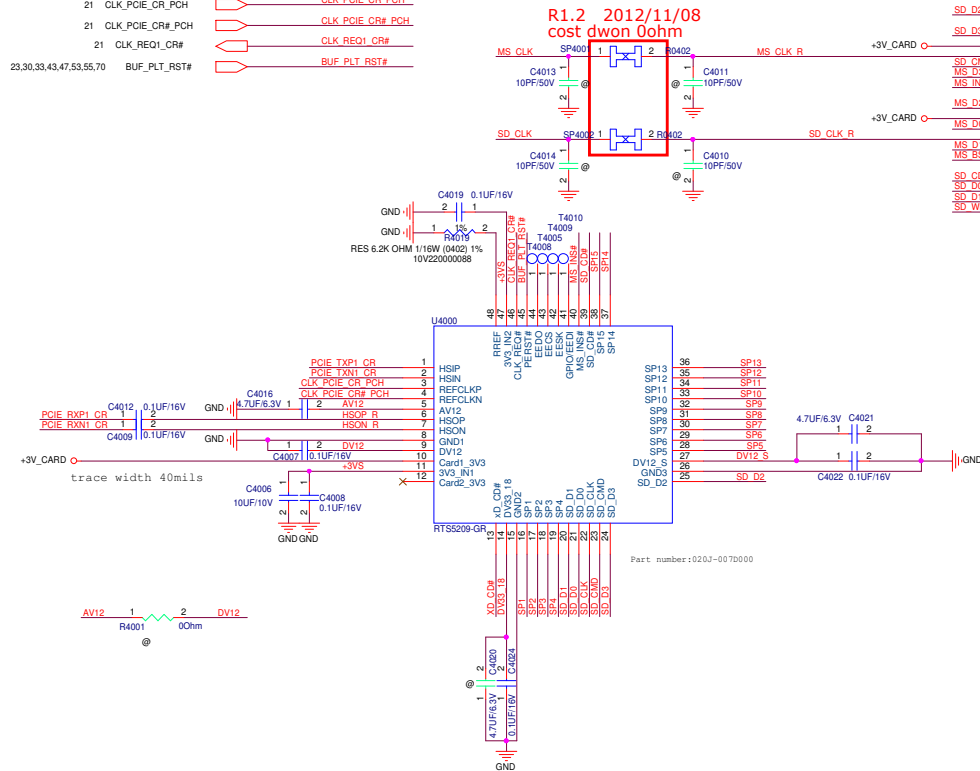
R1.0 0106
HDMI HPD Cost Reduced Level Shifter Design Recommendation



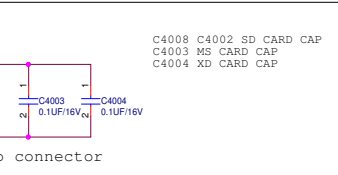
From System's PCIE interface



R1.2 2012/11/08
cost dwon 0ohm



SD/MMC plus/MS/xD



Pin Name	Description
SP1	SD_D7/SD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

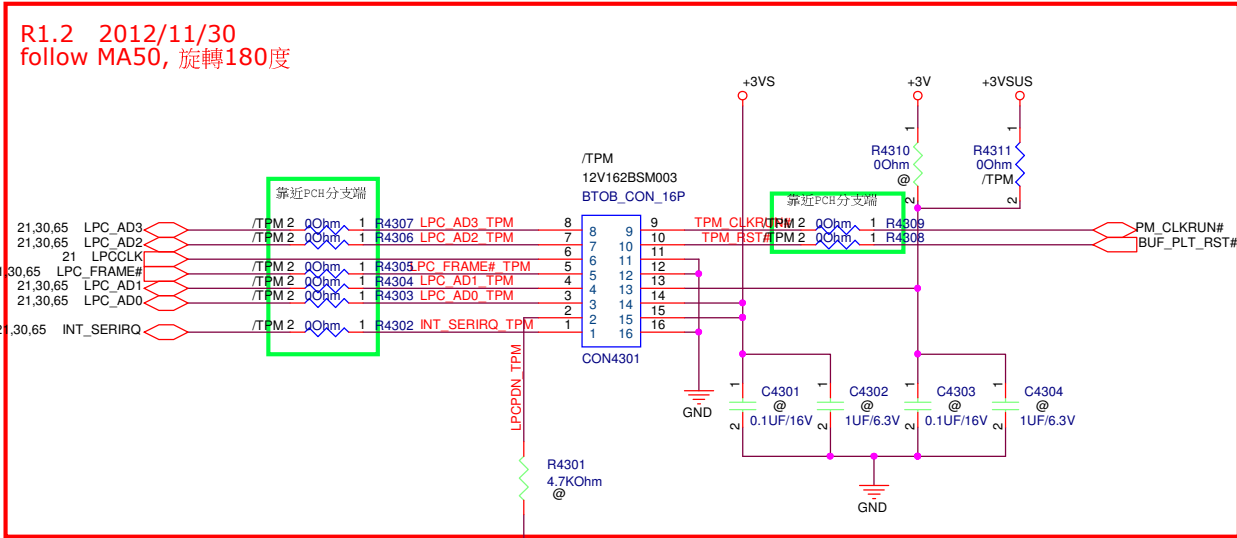
SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Share Pin



Del Entry audio circuit

SR-8
0121-11

PEGATRON		Title : CODEC-ALC269	
ASUSTeK COMPUTER INC. NB1		Engineer: Wing_Cheng	
Size	Project Name		Rev
Custom	VA70_HW		1.0
Date: Friday, January 18, 2013		Sheet	44 of 96

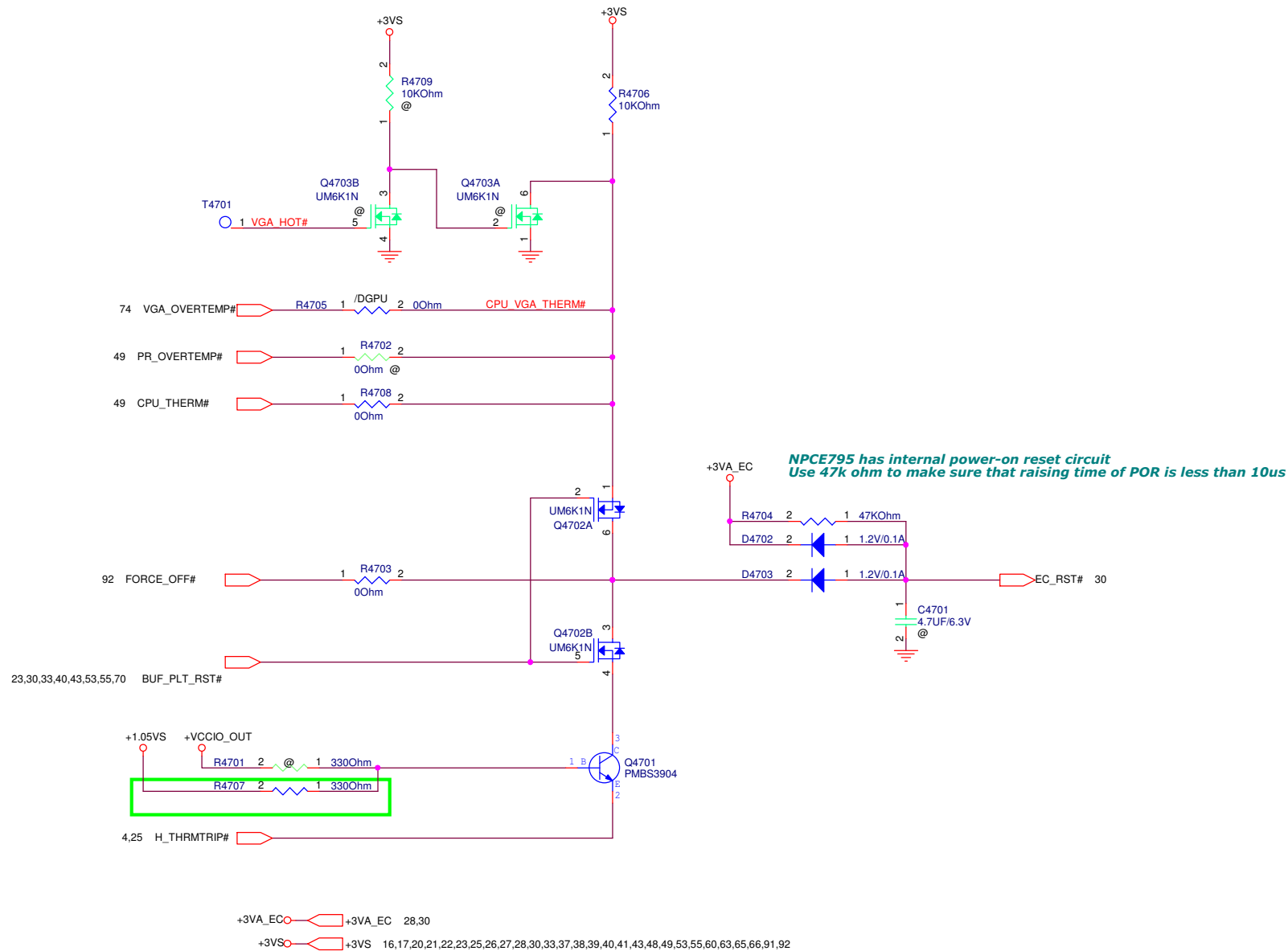


Del Entry audio circuit

SR-8
0121-11

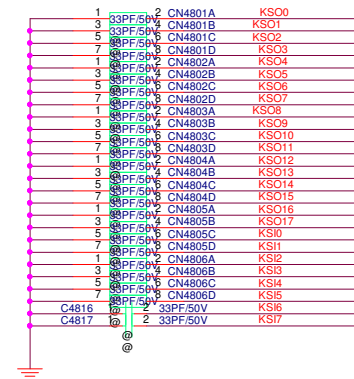
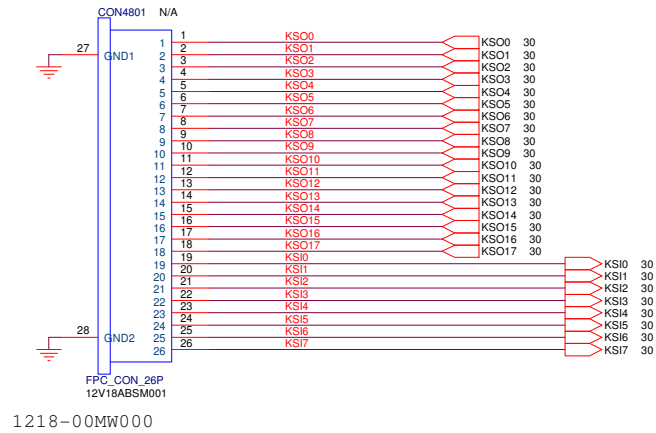
PEGATRON		Title : AUDIO ALC269	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name VA70_HW	Date: Friday, January 18, 2013	Rev 1.0
		Sheet 45 of 96	

Thermal Policy



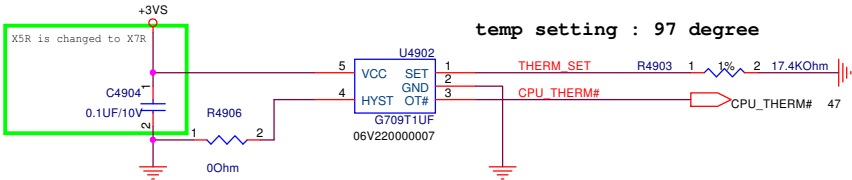
PEGATRON		Title : <u>RST_Reset Circuit</u>	
<u>BG1-HW RD Div.2-NB RD Dept.5</u>		Engineer: <u>Wing_Cheng</u>	
Size B	Project Name VA70_HW		Rev 1.0
Date: <u>Friday, January 25, 2013</u>		Sheet <u>47</u>	of <u>96</u>

Keyboard



U5001 Close to CPU

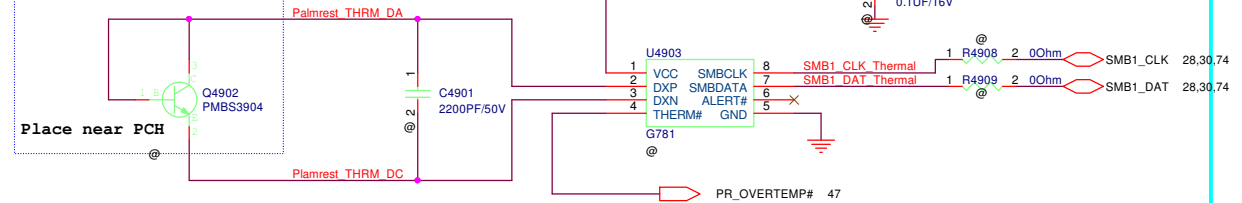
temp setting : 97 degree



Plam Rest Thermal Sensor

PHILIP PMBS3904

Place in the center of Plamrest.



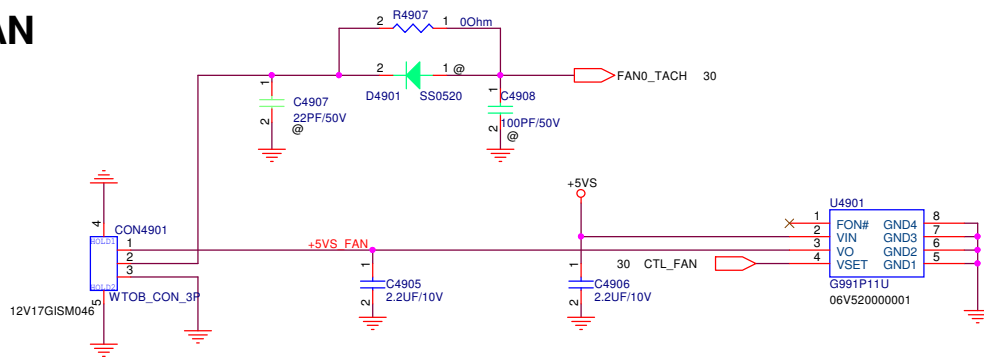
U4903 under palmrest

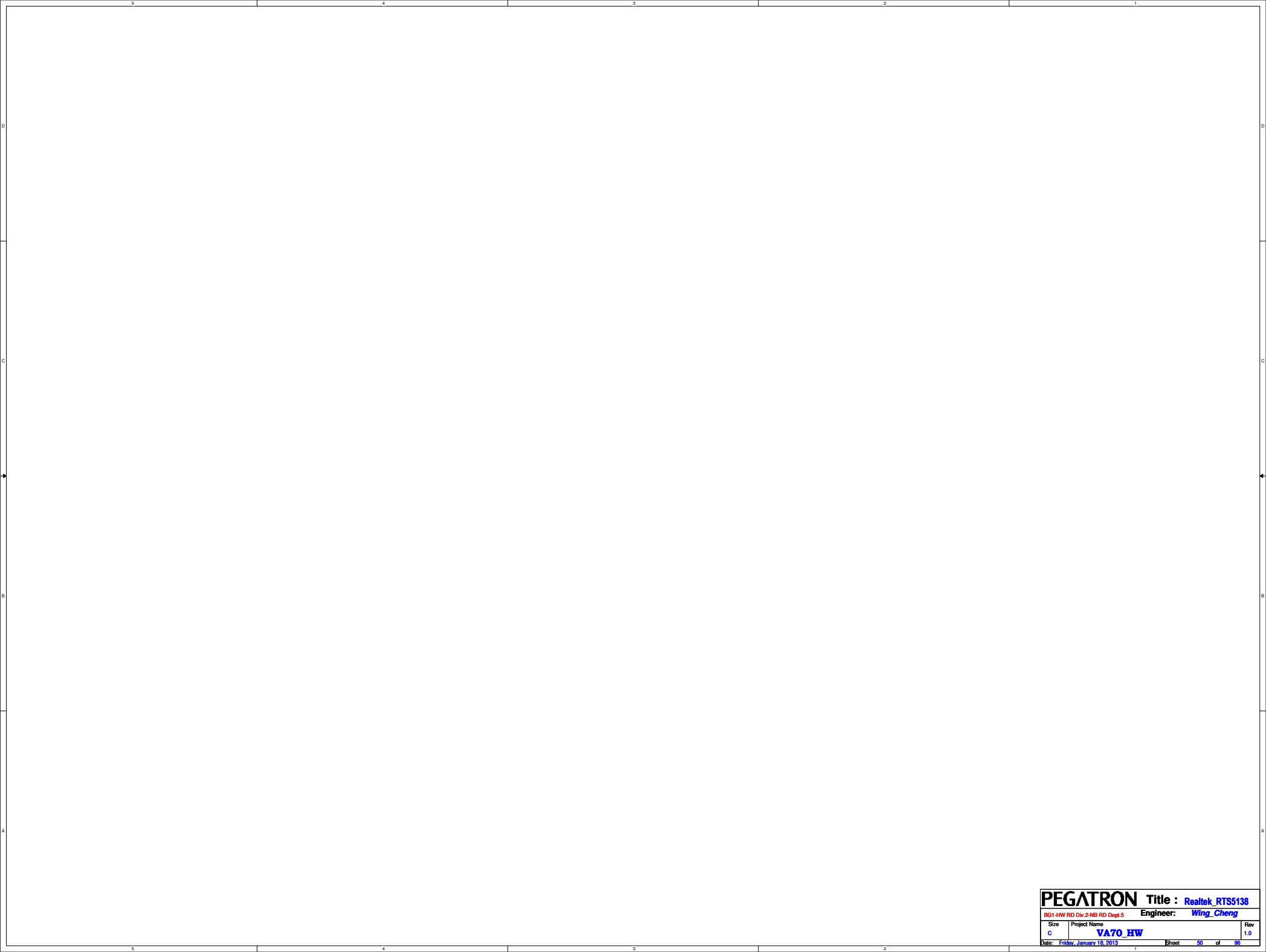
SMBUS addr=1001100x (98)

U4903: Remote(Local) thermal sensor,use remote mode.

R1.2-10

FAN





PEGATRON		Title : Realtek_RT55138	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Wing_Cheng	
Size C	Project Name VA70_HW	Rev 1.0	
Date: Friday, January 18, 2013		Sheet 50 of 95	

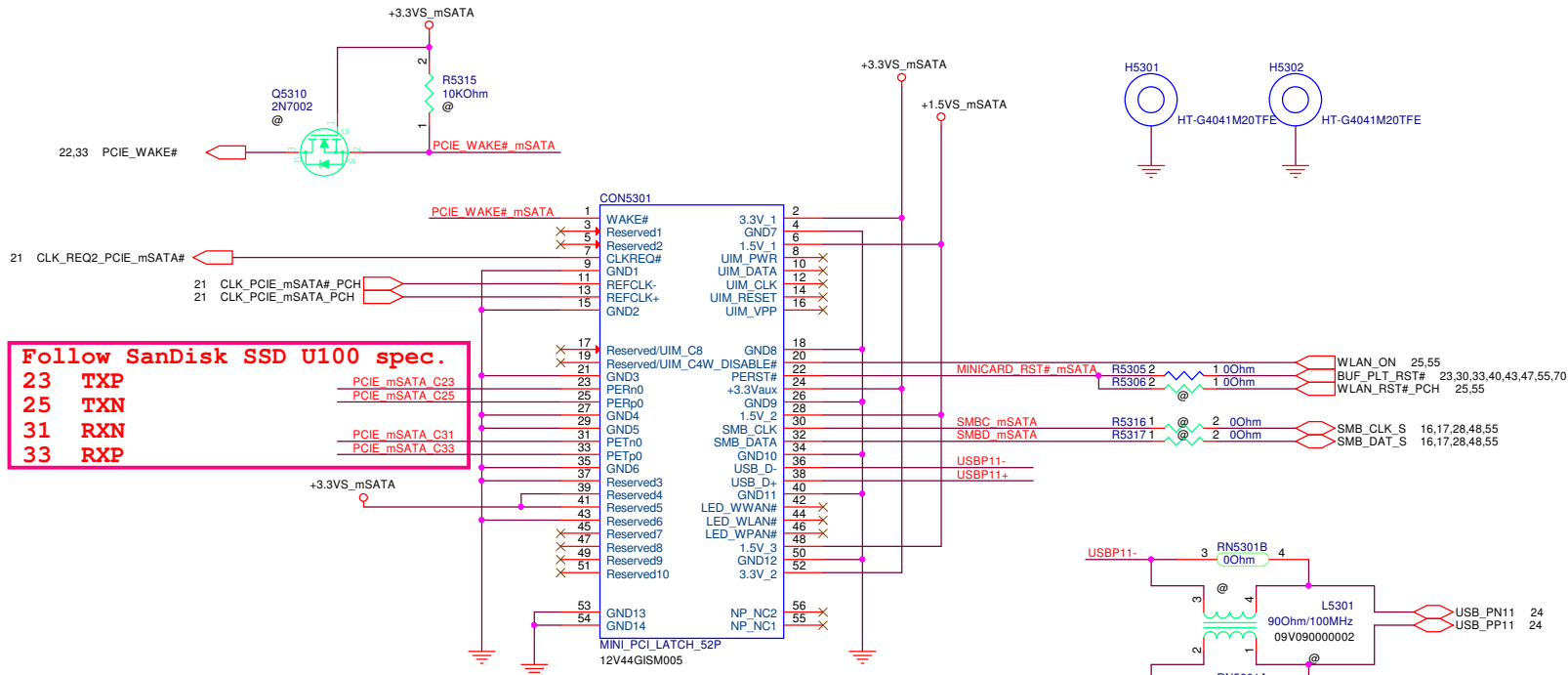
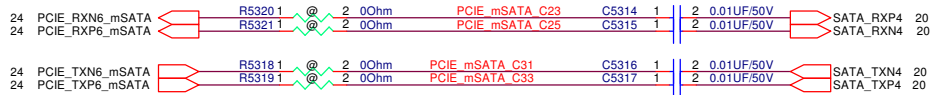




PEGATRON		Title : PCIE NEW CARD	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Wing_Cheng</i>	
Size	Project Name		Rev
Custom	VA70_HW		1.0
Date: Friday, January 18, 2013		Sheet	52 of 96

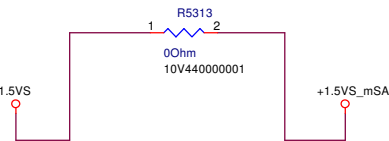
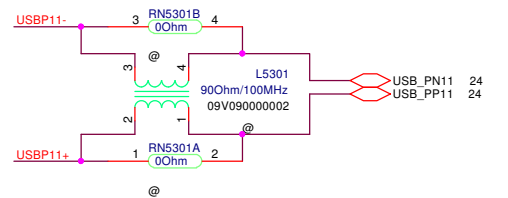
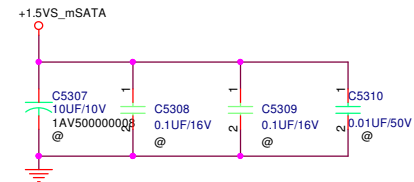
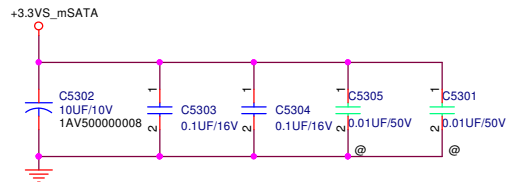
PCIE/mSATA

Select PCIE or mSATA IF select mSATA (only +3VAUX)



Follow SanDisk SSD U100 spec.

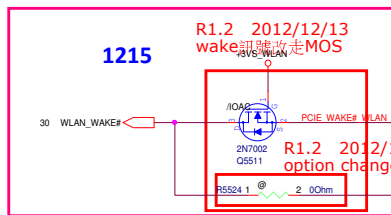
23 TXP
25 TXN
31 RXN
33 RXP



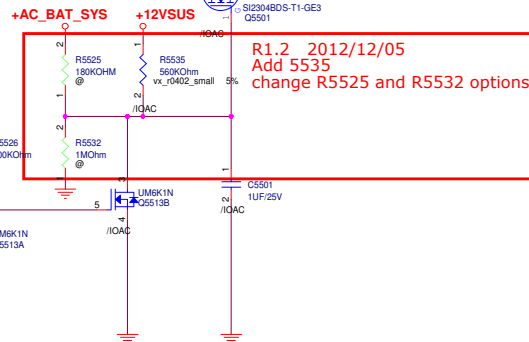
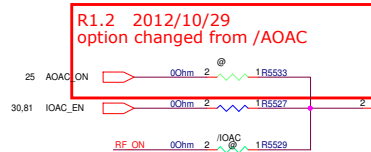
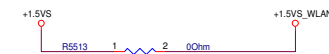
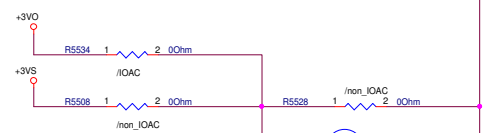
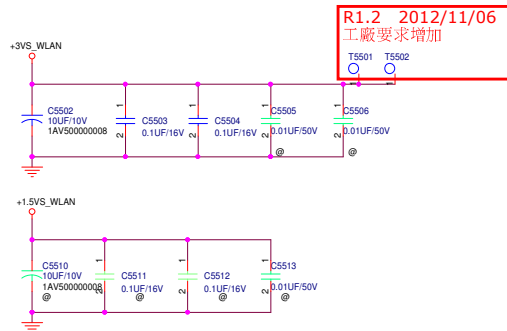
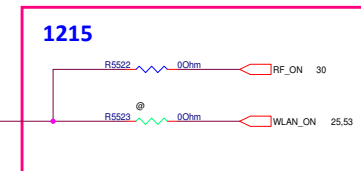
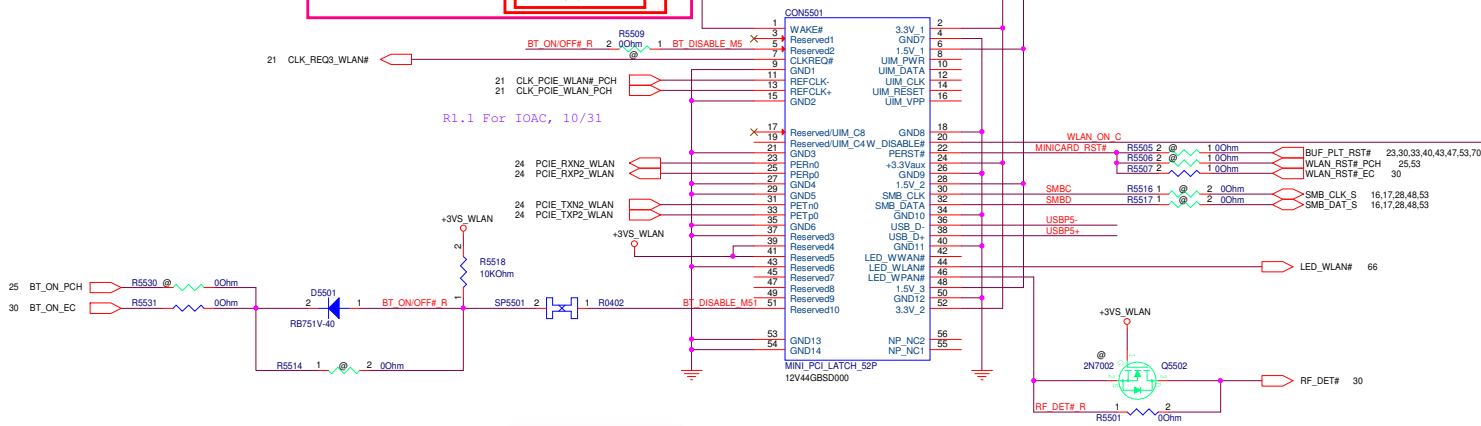
PEGATRON Title : WIF/WIMAX	
BU1-RD Div.1-HW RD Dept.1 Engineer:	
Size	Project Name
Custom	VA70_HW
Date: Friday, January 18, 2013	Sheet 53 of 96

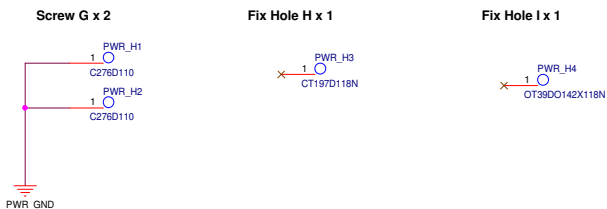


PEGATRON		Title : MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Wing_Cheng</i>	
Size	Project Name		Rev
Custom	VA70_HW		1.0
Date: Friday, January 18, 2013		Sheet	54 of 96

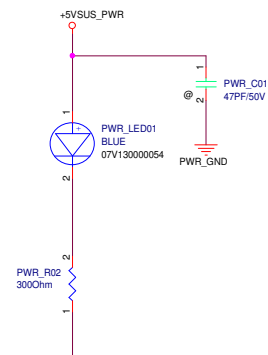


WIFI/WiMAX

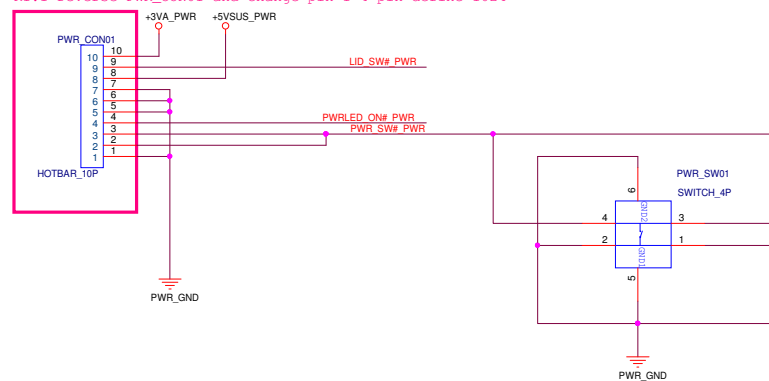




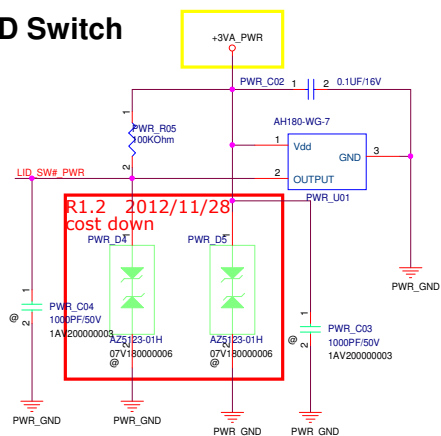
POWER Button LED

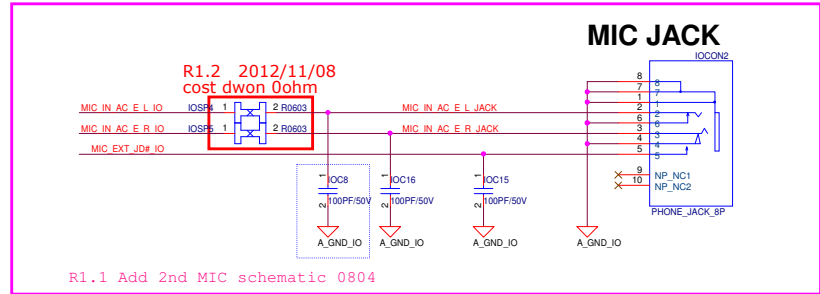
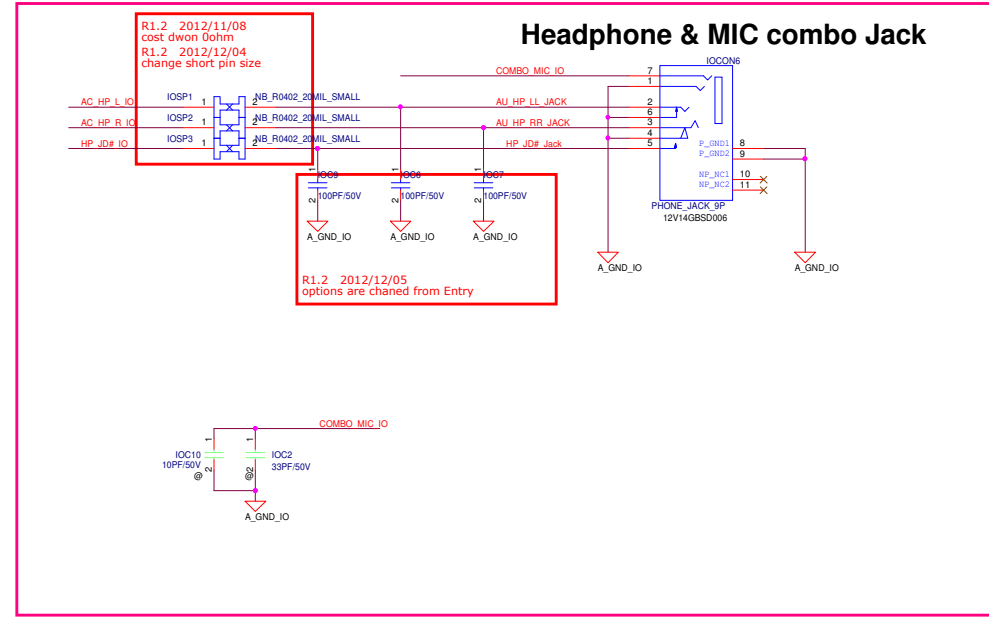
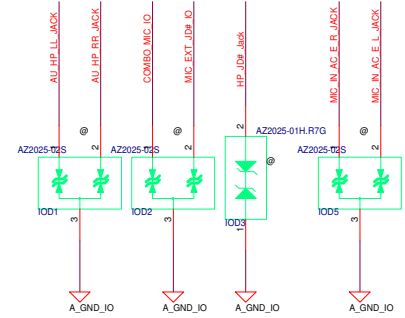
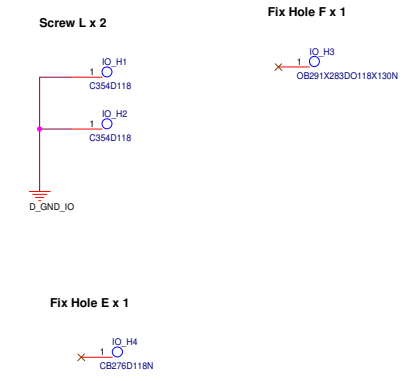
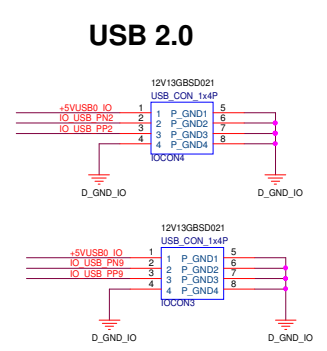
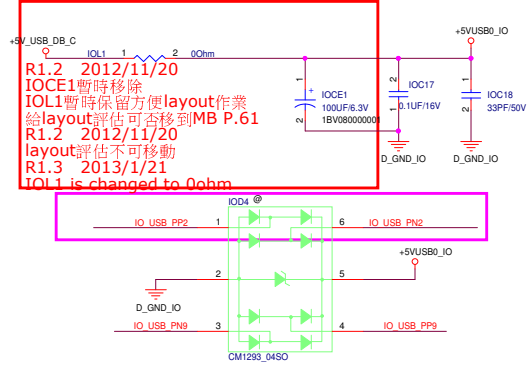
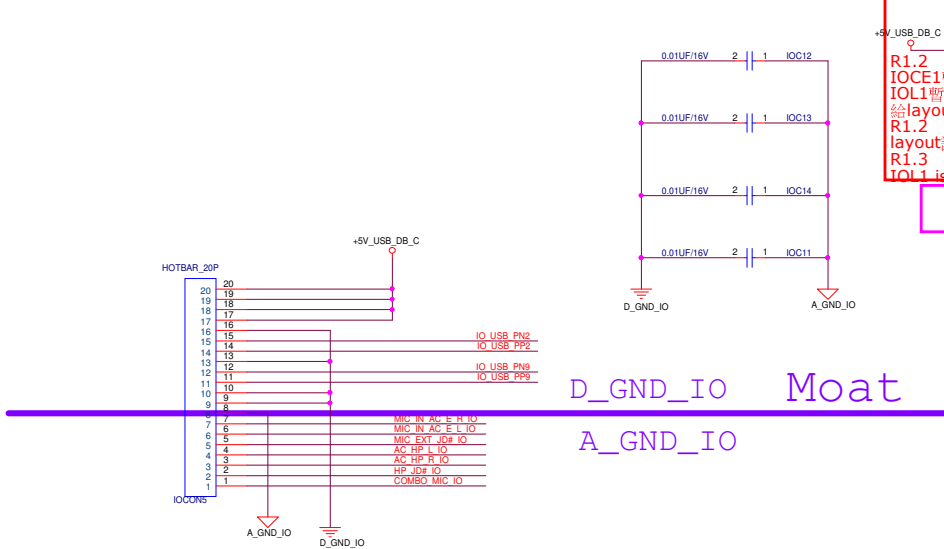


R1.1 reverse PWR_CON01 and change pin 1~4 pin define 1024



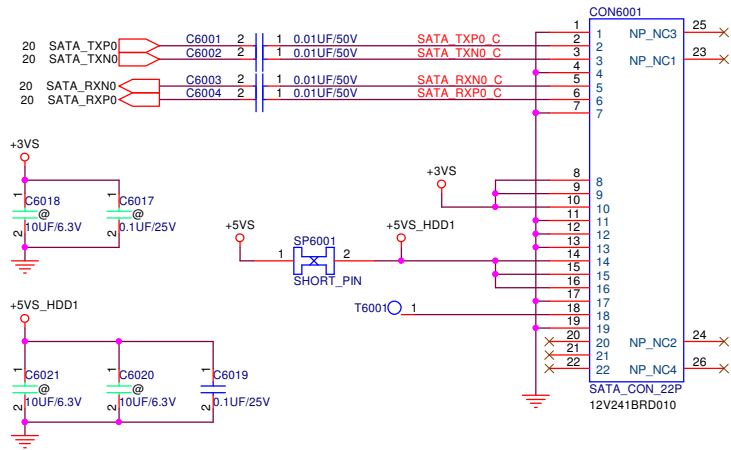
LID Switch





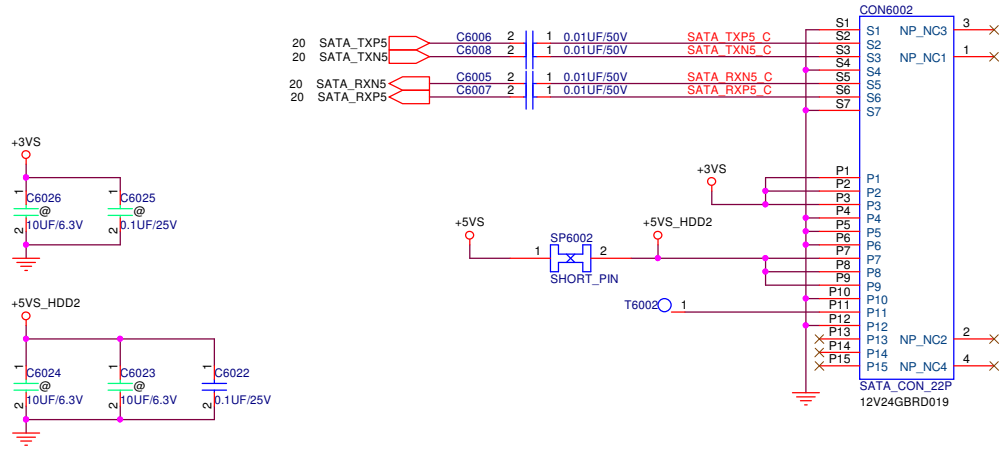
HDD 1

9.5mm



HDD 2

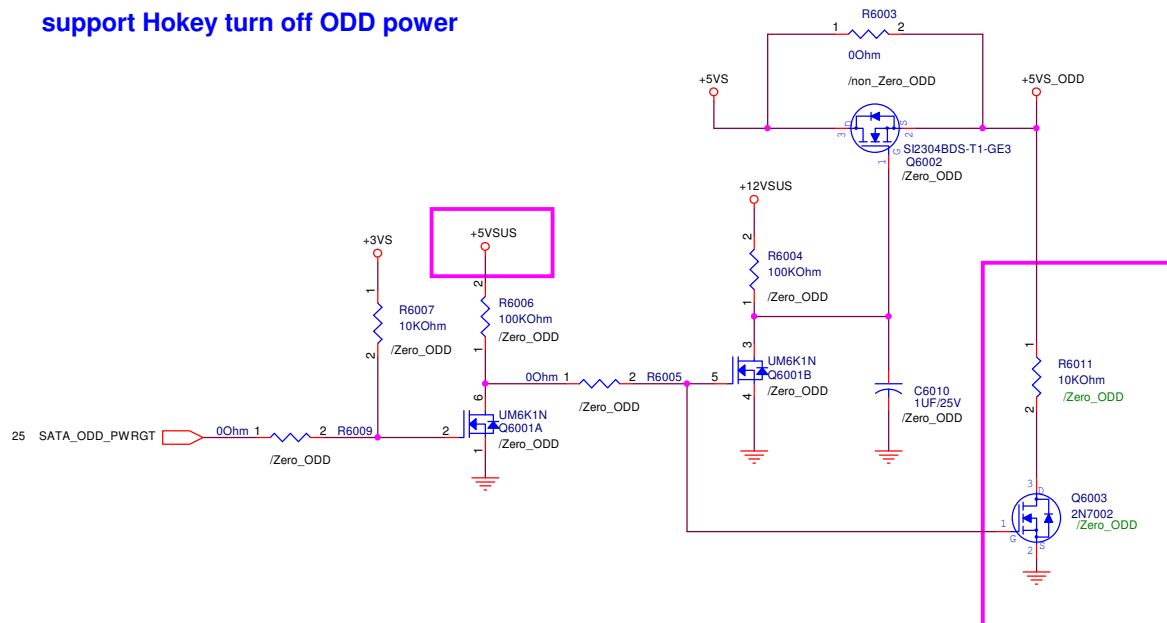
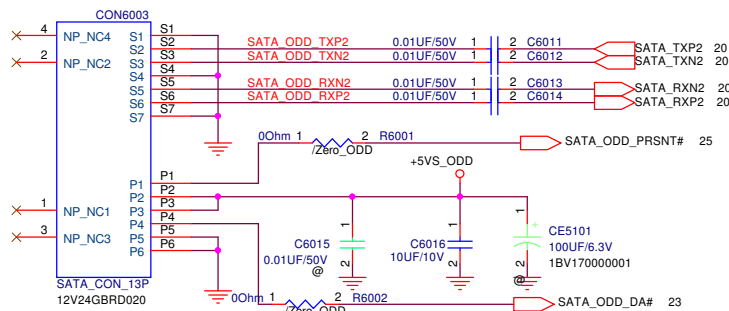
12.5mm



ODD

ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



PEGATRON Title : SATA HDD/ ODD

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing Cheng

Size

Project Name

Custom

VA70_HW

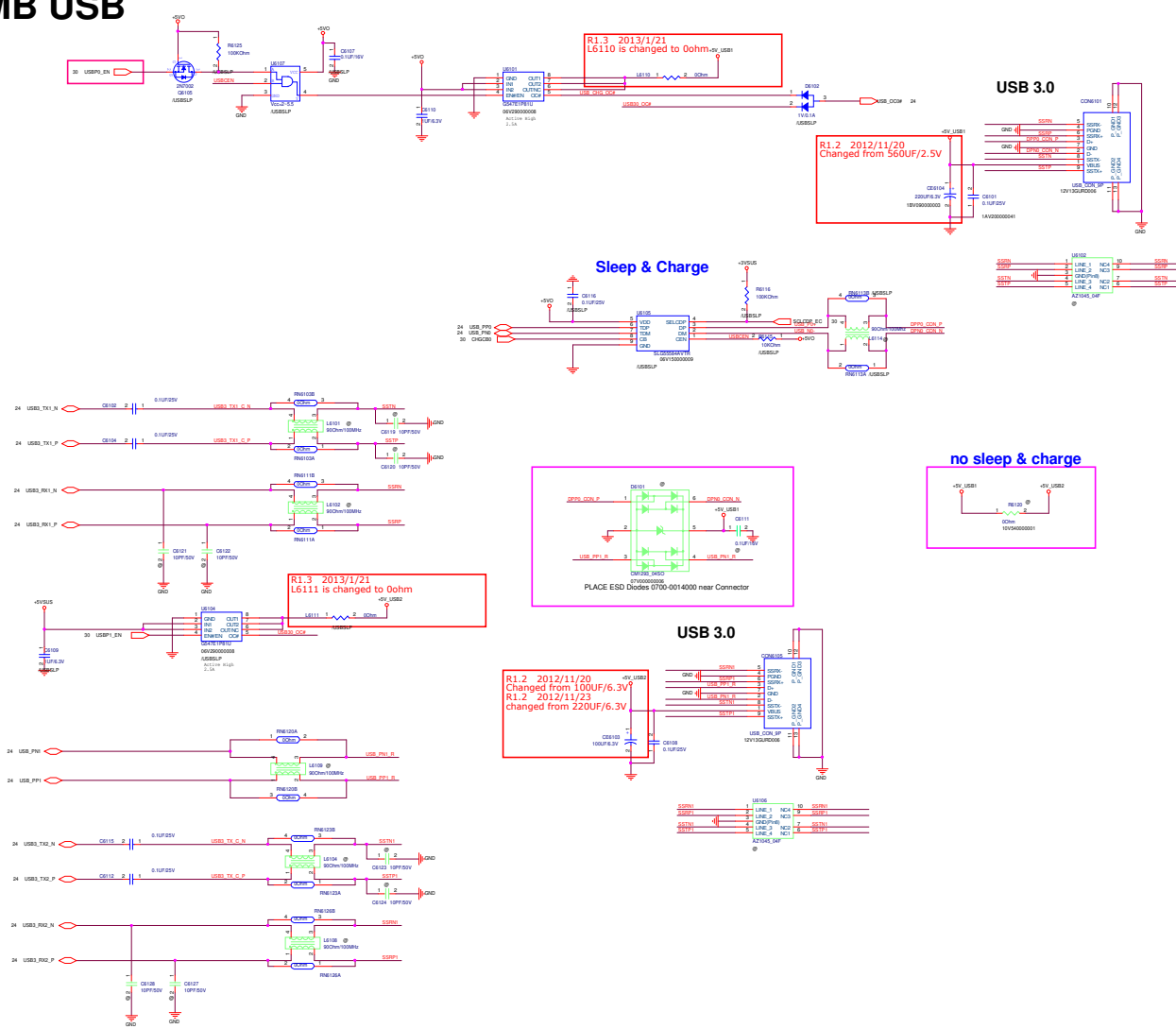
Rev

1.0

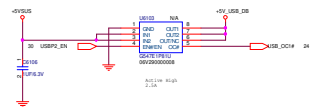
Date: Friday, January 18, 2013

Sheet 60 of 96

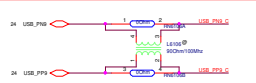
MB USB



IO Board

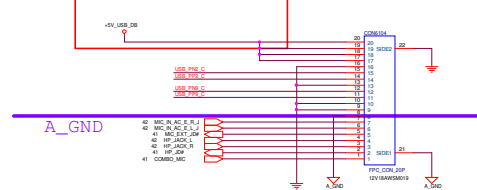


BIOS debug port



AUDIO BOARD/w USB2.0 x2

R1.2 2012/11/20
Add 560UF/2.5V for layout to estimate
R1.2 2012/11/23
changed from 560/2.5V
R1.2 2012/11/27
L6115, CE6105 are removed

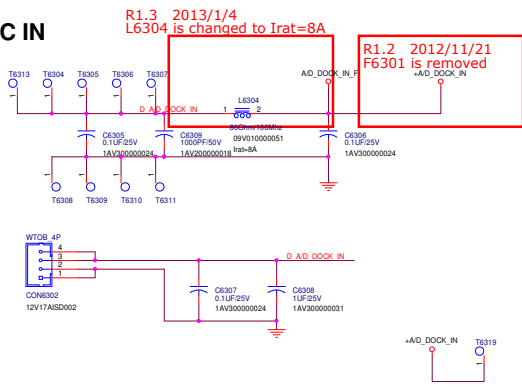




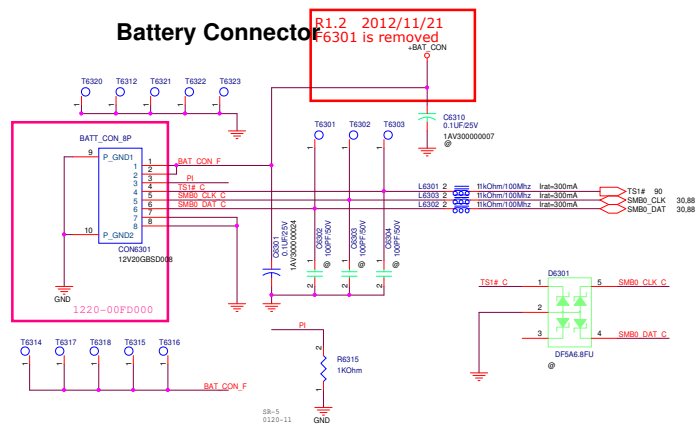
WWW.AliSaler.Com

PEGATRON		Title : Camera/ BT/ FL CONN	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name VA70_HW		Rev 1.0
Date: Friday, January 18, 2013		Sheet	62 of 96

DC IN

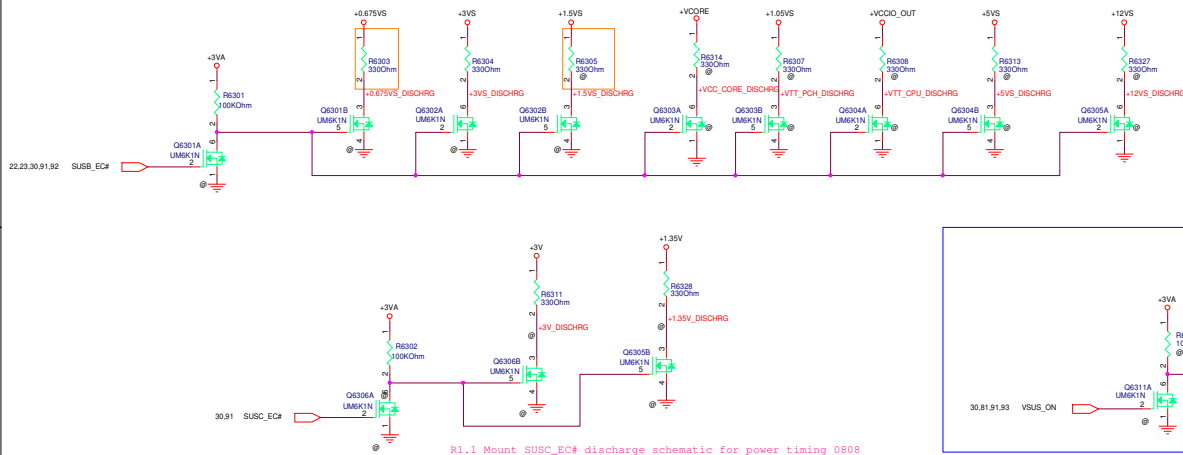


Battery Connector

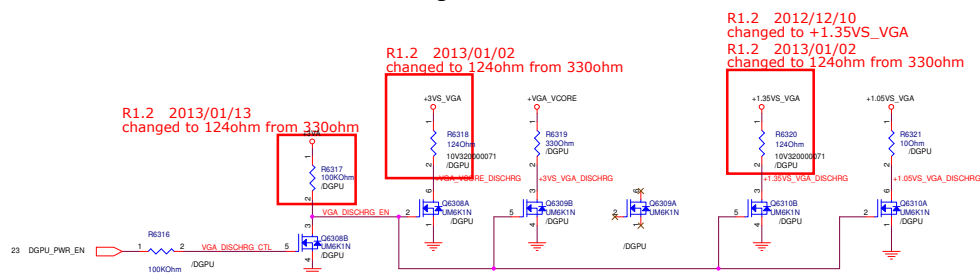


Discharge Circuit

Frank
0505 Follow EVEREST

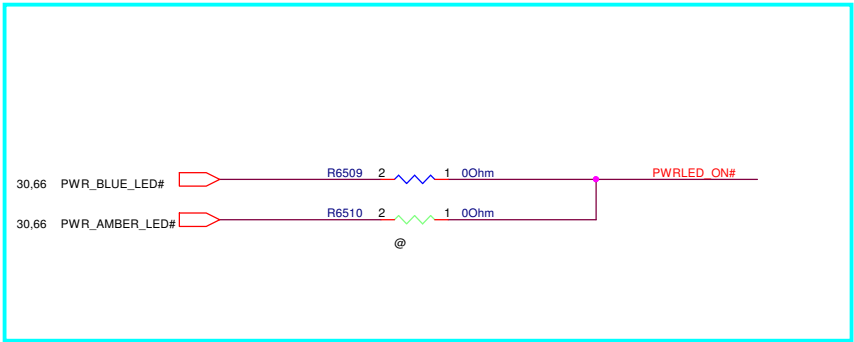
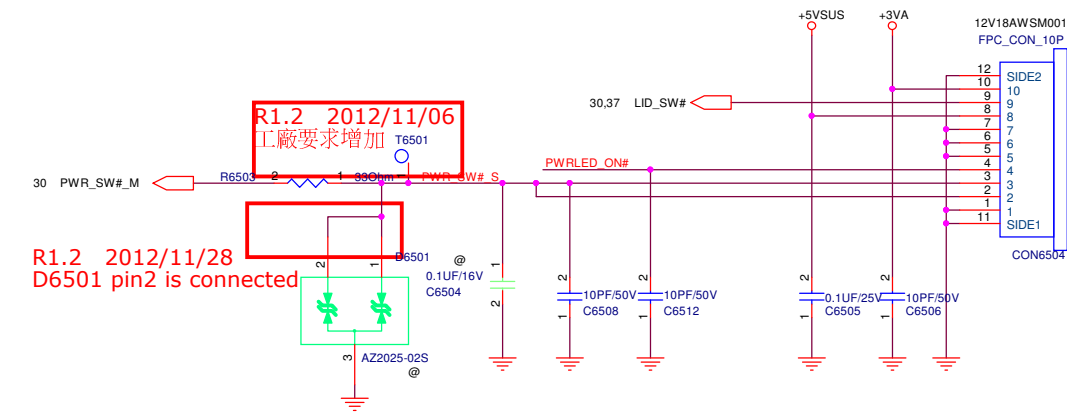


VGA Discharge Circuit



Unmount +VGA_Vcore discharg

PWR BRD/ AMBIENT/ HALL CONN.

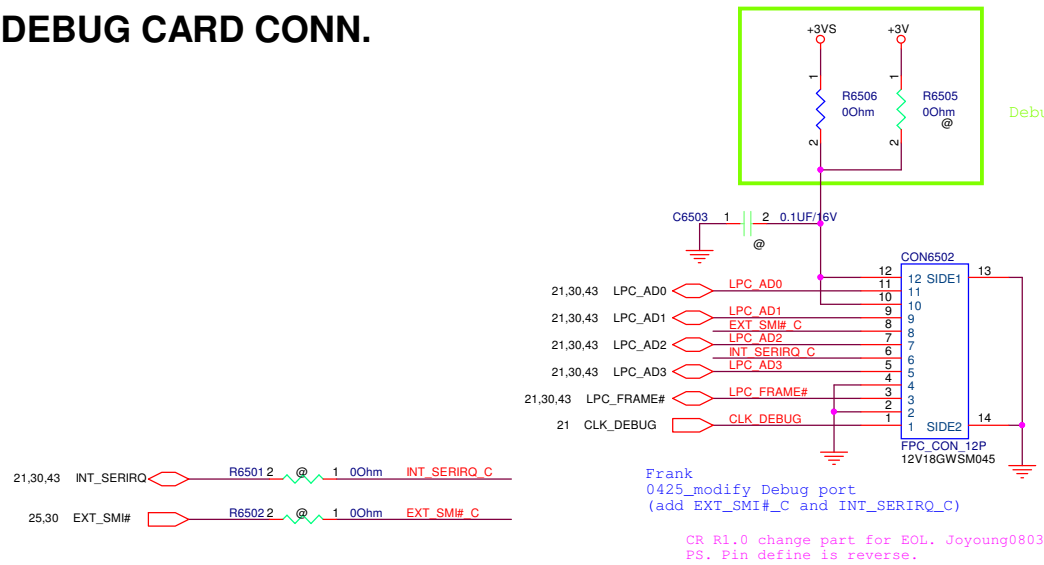


R1.2-28

change Power LED CON6503 circuit

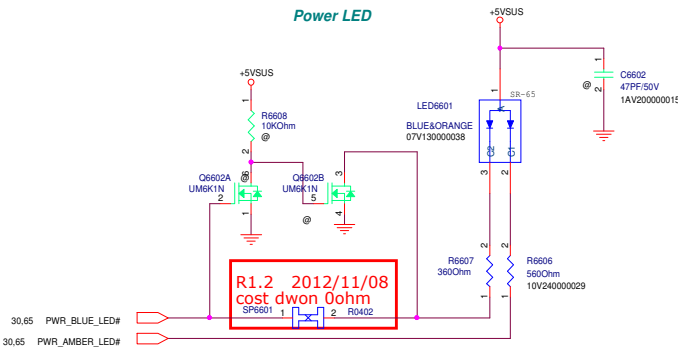
R1.0 remove VG70 POWER connector CON6503 0719

DEBUG CARD CONN.

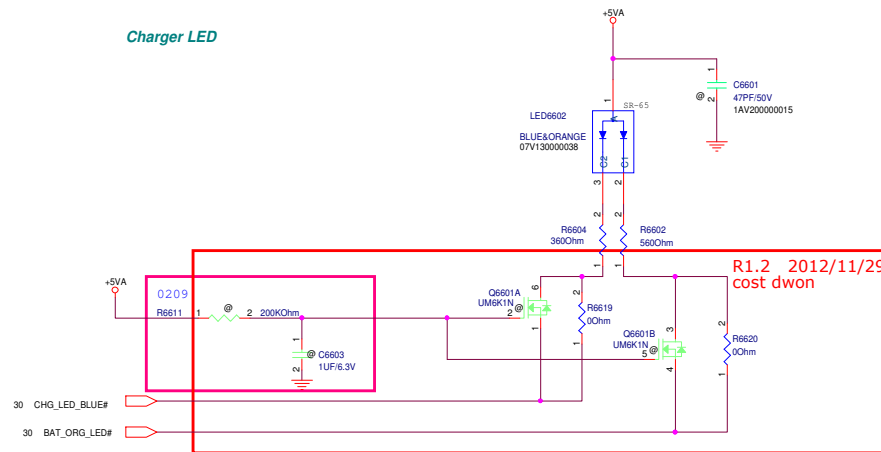


Frank
0425_modify Debug port
(add EXT_SMI#_C and INT_SERIRQ_C)
CR R1.0 change part for EOL. Joyoung0803
PS. Pin define is reverse.

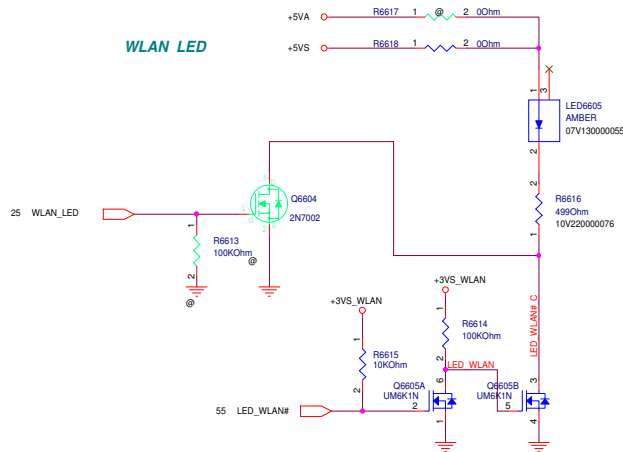
Power LED



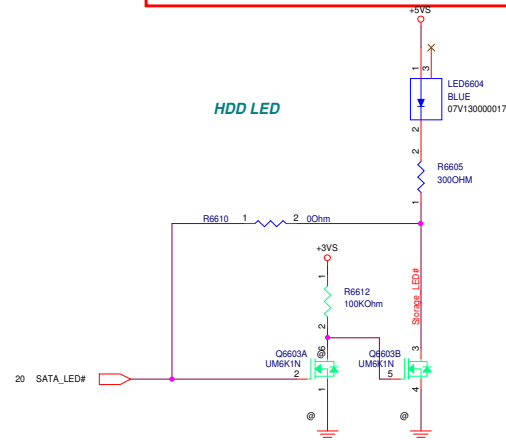
Charger LED



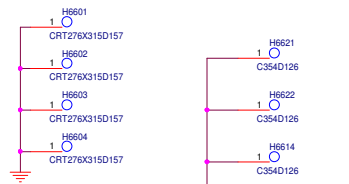
WLAN LED



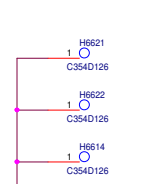
HDD LED



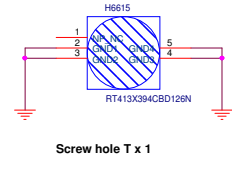
CPU Screw B x 4



Screw A x 4 (PTH)



Screw hole R x 1



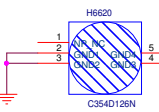
Screw hole T x 1



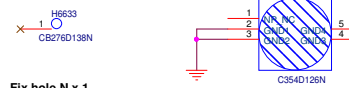
GPU Screw P x 2



Screw A x 2 (NPTH)



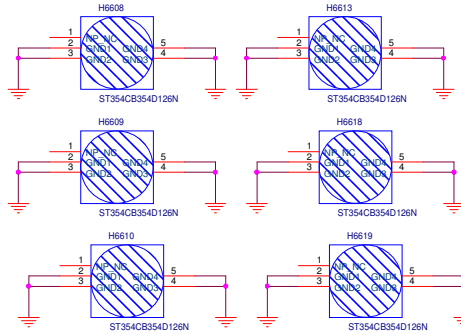
Fix hole D x 1



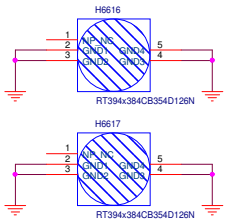
Fix hole N x 1



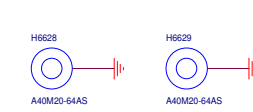
Screw hole Q x 6



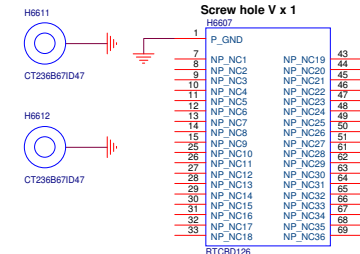
Screw hole S x 2



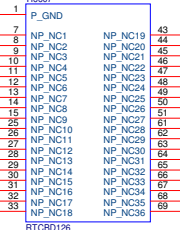
WLAN NUT



PCH Local Side Symbol



Screw hole V x 1



D

C |

B

A

PEGATRON Title : Finger Printer

Pegatron Corp.

Engineer: *Wing_Cheng*

Size
A

Project Name	
--------------	--

VA70_HW

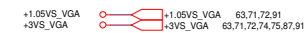
Rev
1.0

Date: Friday, January 18, 2013

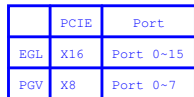
Sheet 68 of 96

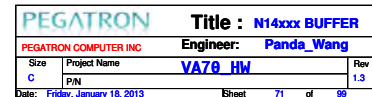
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

PEGATRON Title : G-Sensor TSH35TR		
BU1-RD Div.1-HW RD Dept.1 Engineer: Wing_Cheng		
Size A	Project Name	Rev 1.0
Date: Friday, January 18, 2013		Sheet 69 of 96



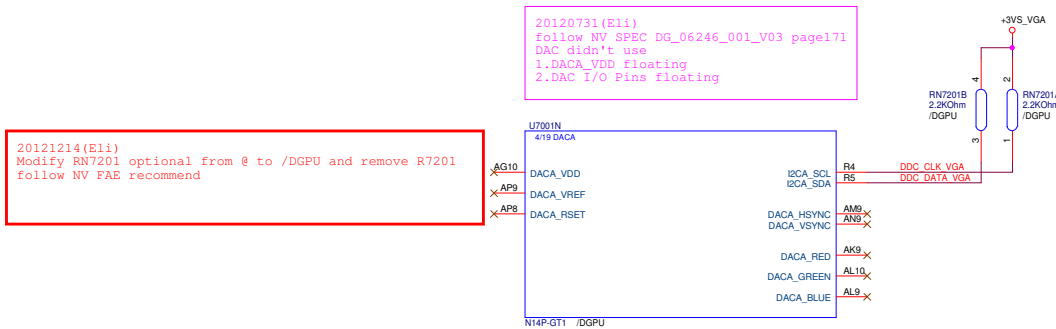
```
| @ => Unmount.  
| /DGPU => Optimus SKU.  
| /EGL => When N14E-GL is mounted, we need to mount this optional.  
| /PGV => When N14P-GV is mounted, we need to mount this optional.  
| /EGL_PGV => When N14E-GL or N14P-GV are mounted, we need to mount this optional.
```



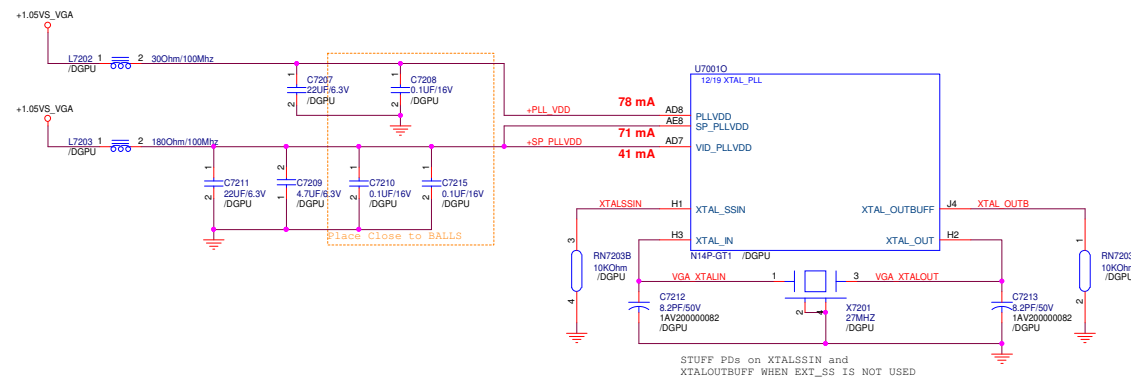


VGA

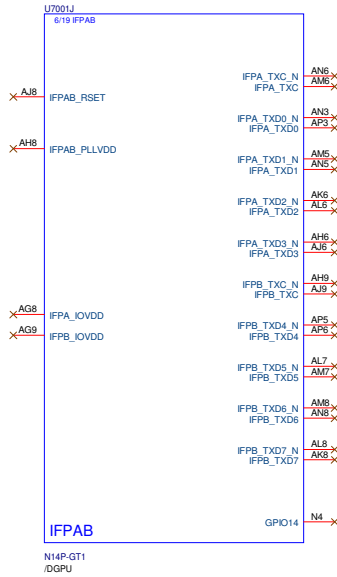
+1.05VS_VGA 63,70,71,91
+3VS_VGA 63,70,71,74,75,87,91



X ' TAL

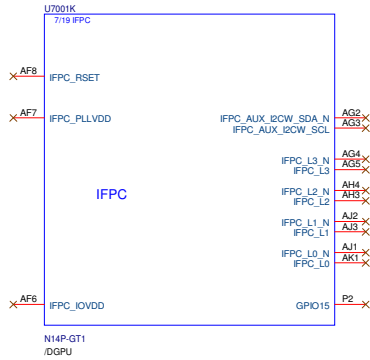


LVDS

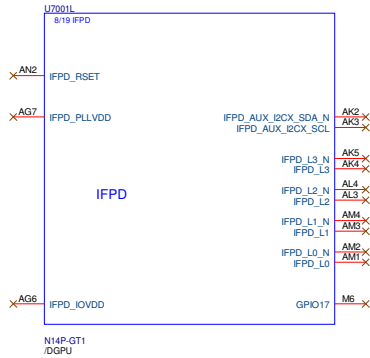


20121214(E11)
Remove R7303, R7304, R7305, R7306, R7308, R7309, R7310,
R7312, RN7301, RN7302 follow NV FAE recommend

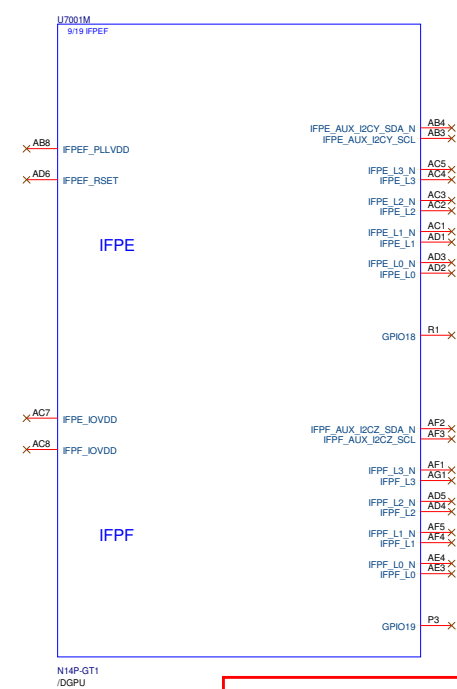
HDMI



eDP



DVI



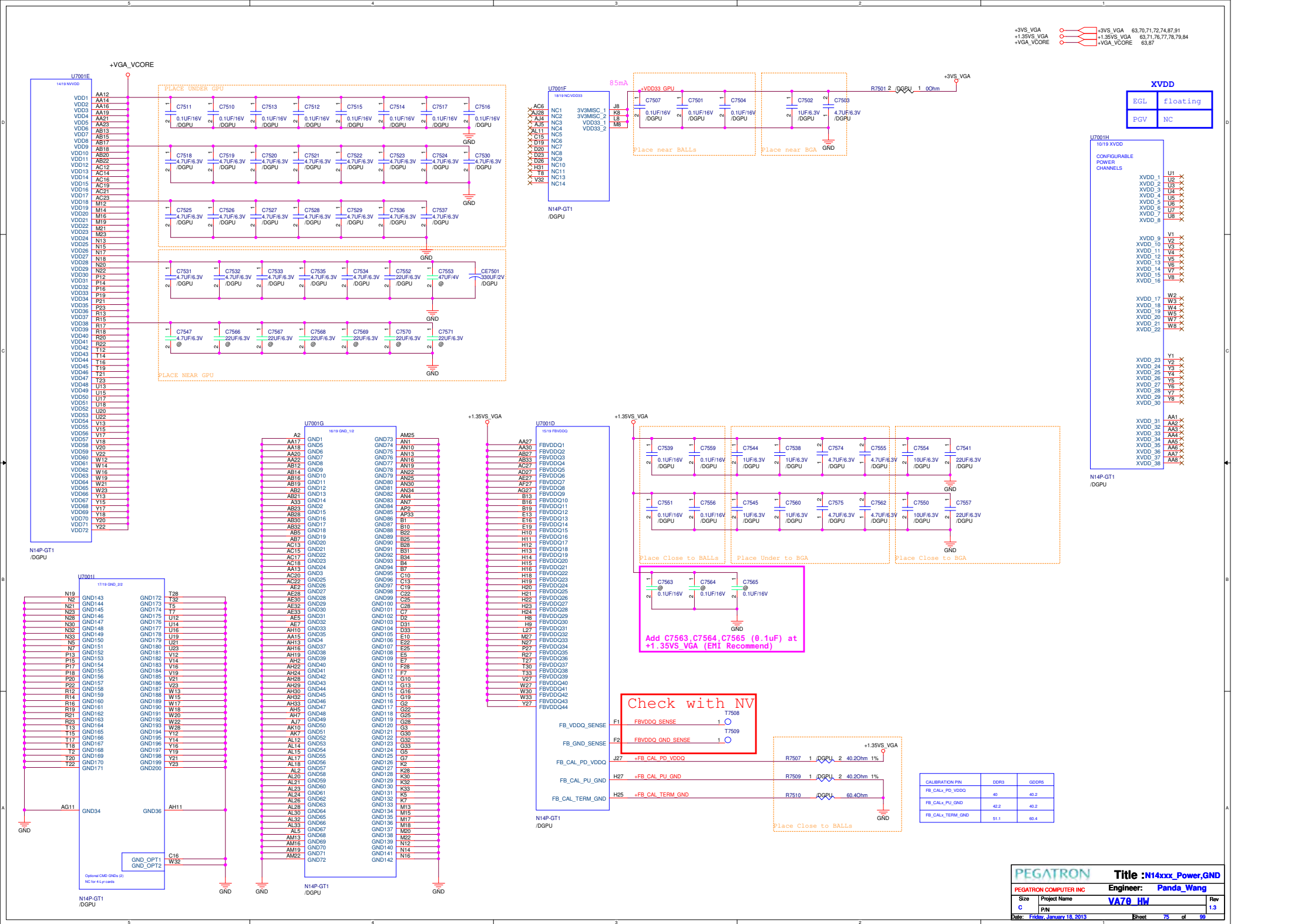
20121221(E11)
Remove T7301, T7302, T7303, T7304 follow NV FAE recommend

IFPX channel

	N14E-GL Standard Mode	N14P-GV Combined Mode
IFPA	LVDS	LVDS(DP/DVI)
IFPB	LVDS	LVDS(DP/DVI)
IFPC	DP/HDMI	DP/HDMI
IFPD	DP/eDP	DP/eDP
IFPE	DP/DVI	X
IFPF	DP/DVI	X

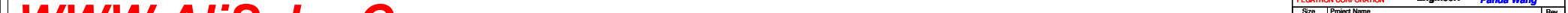
GPIO Definition

	NV SPEC Standard mode DG_06246_001_V03	VA70_HW
GPIO14	IFPAB_HPD (LVDS)	NC
GPIO15	IFPC_HPD (HDMI)	NC
GPIO17	IFPD_HPD (eDP)	NC
GPIO18	IFPE_HPD (DVI)	NC
GPIO19	IFPF_HPD (DVI)	NC

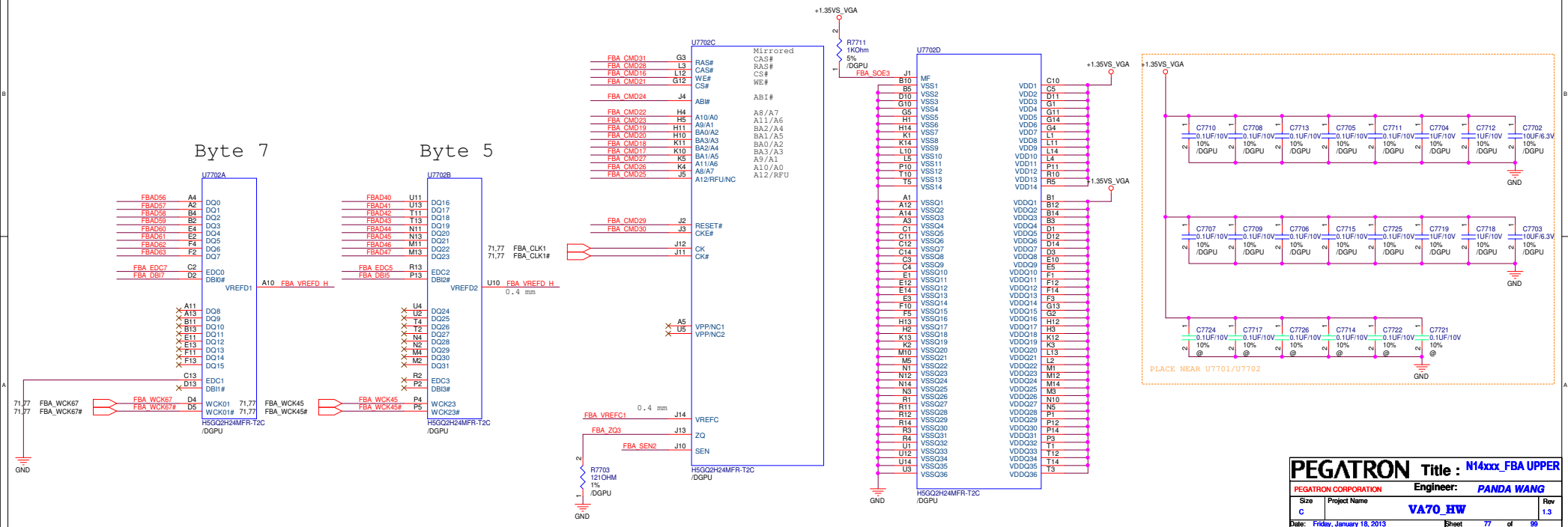
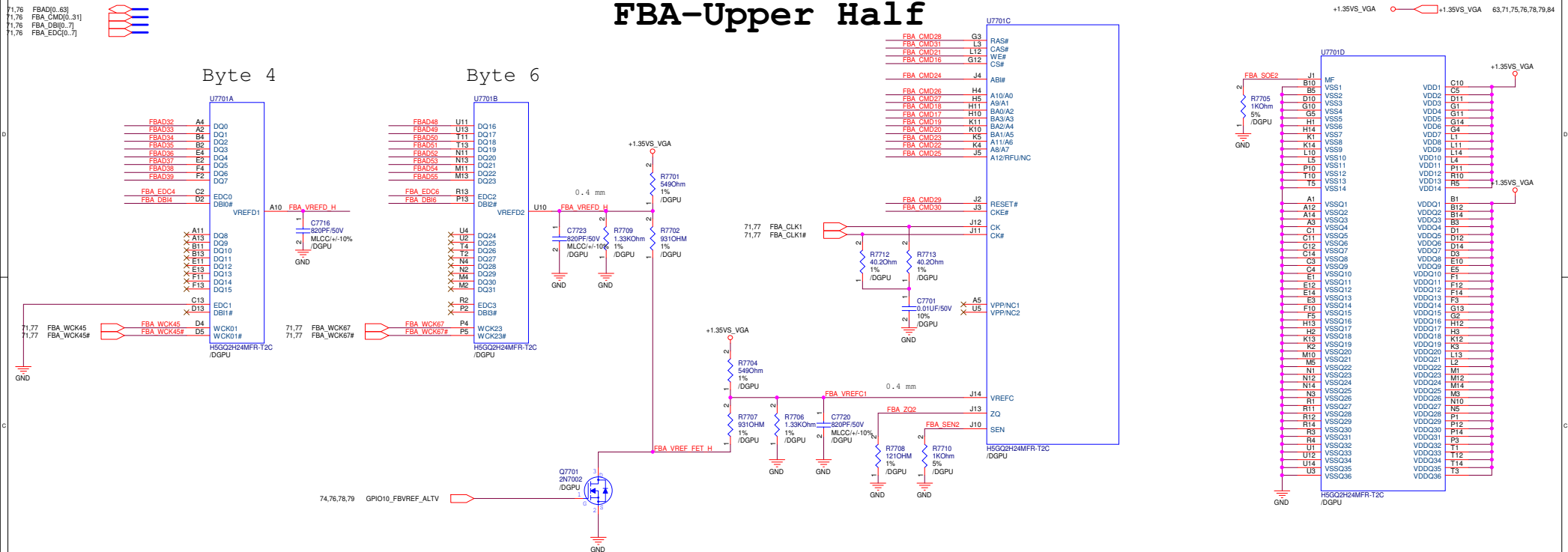


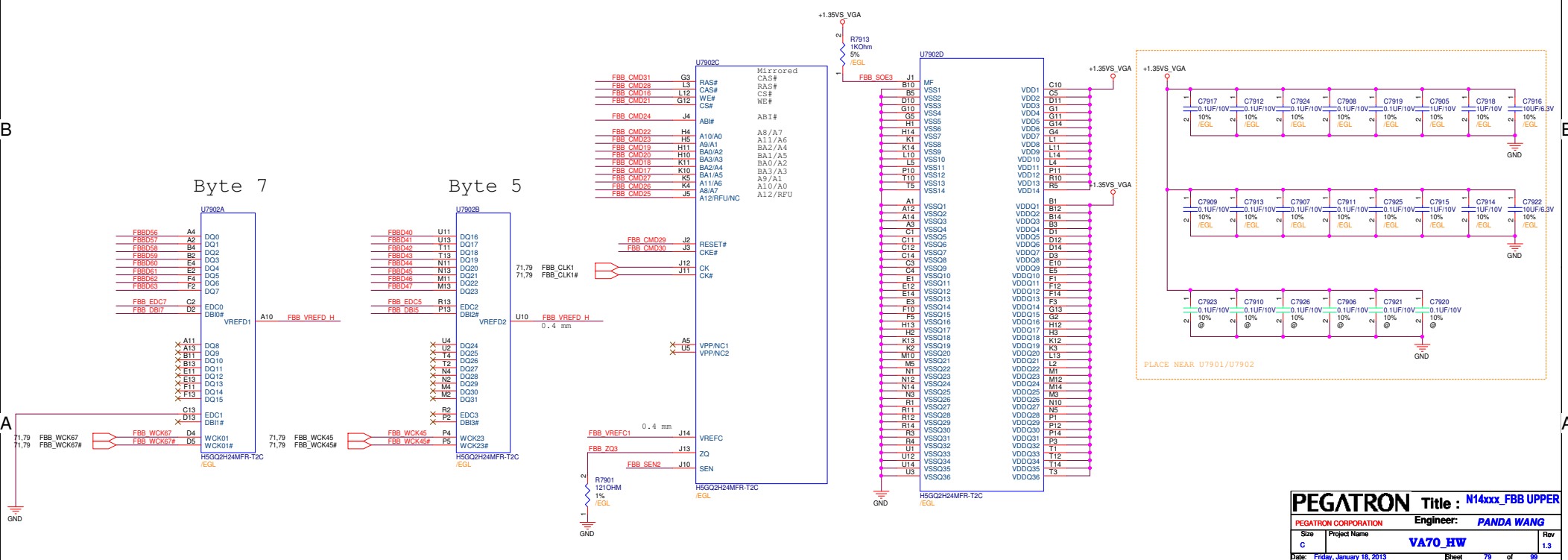
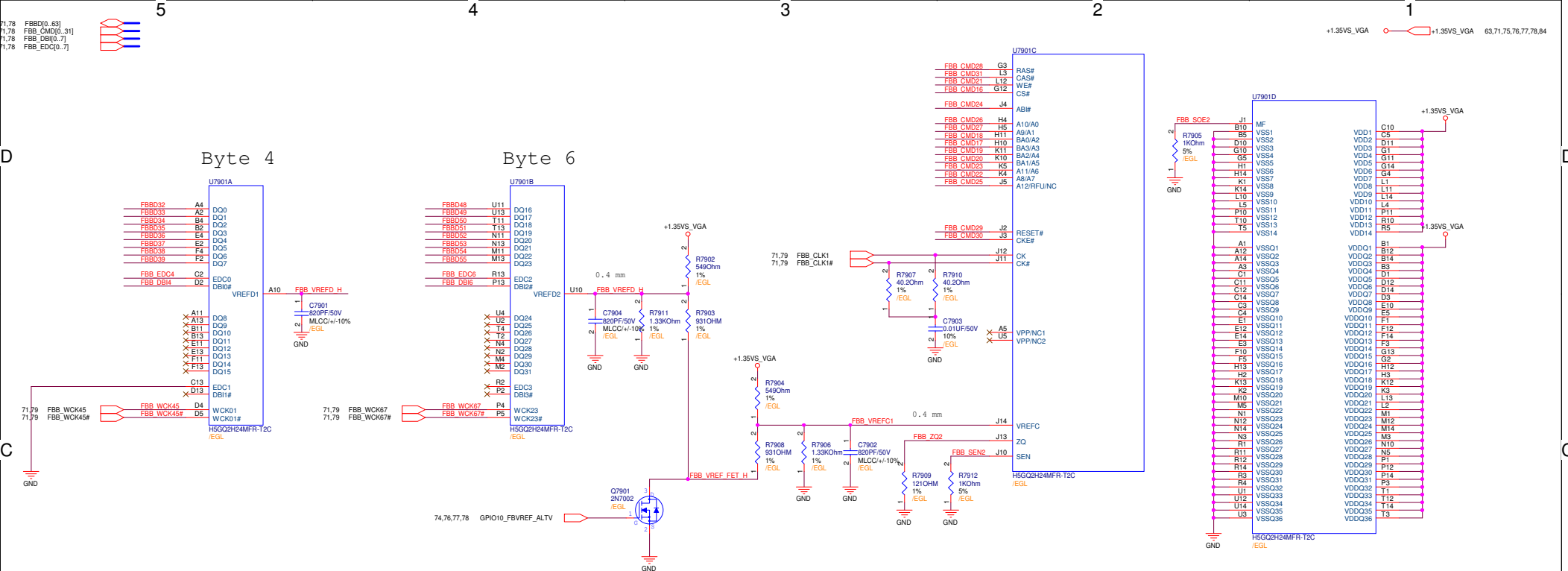
+1.35VS_VGA +1.35VS_VGA 63,71,75,77,78,79,84

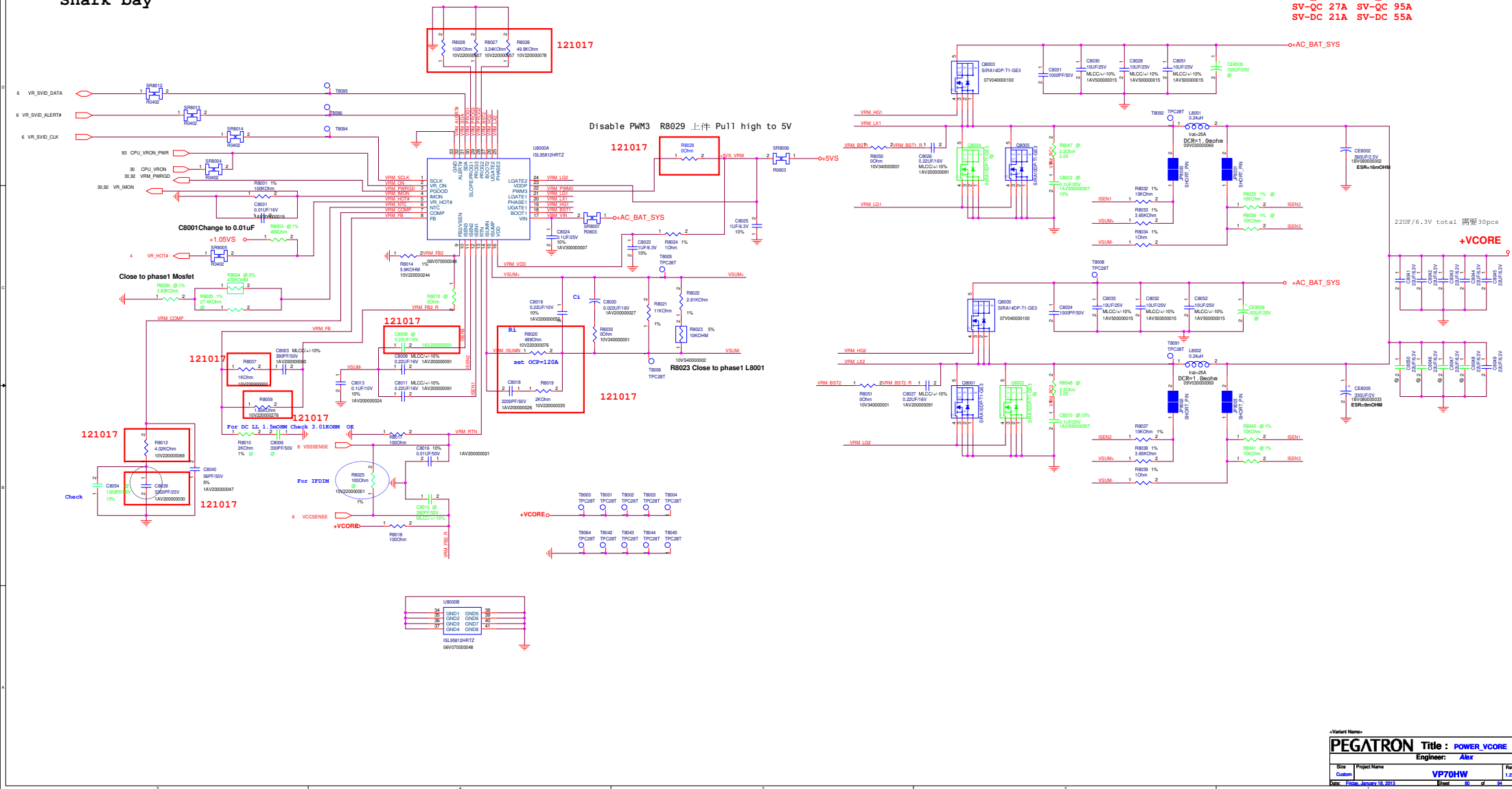
Byte 2



FBA-Upper Half







-Variant Name-

PEGATRON Title : POWER_VCORE

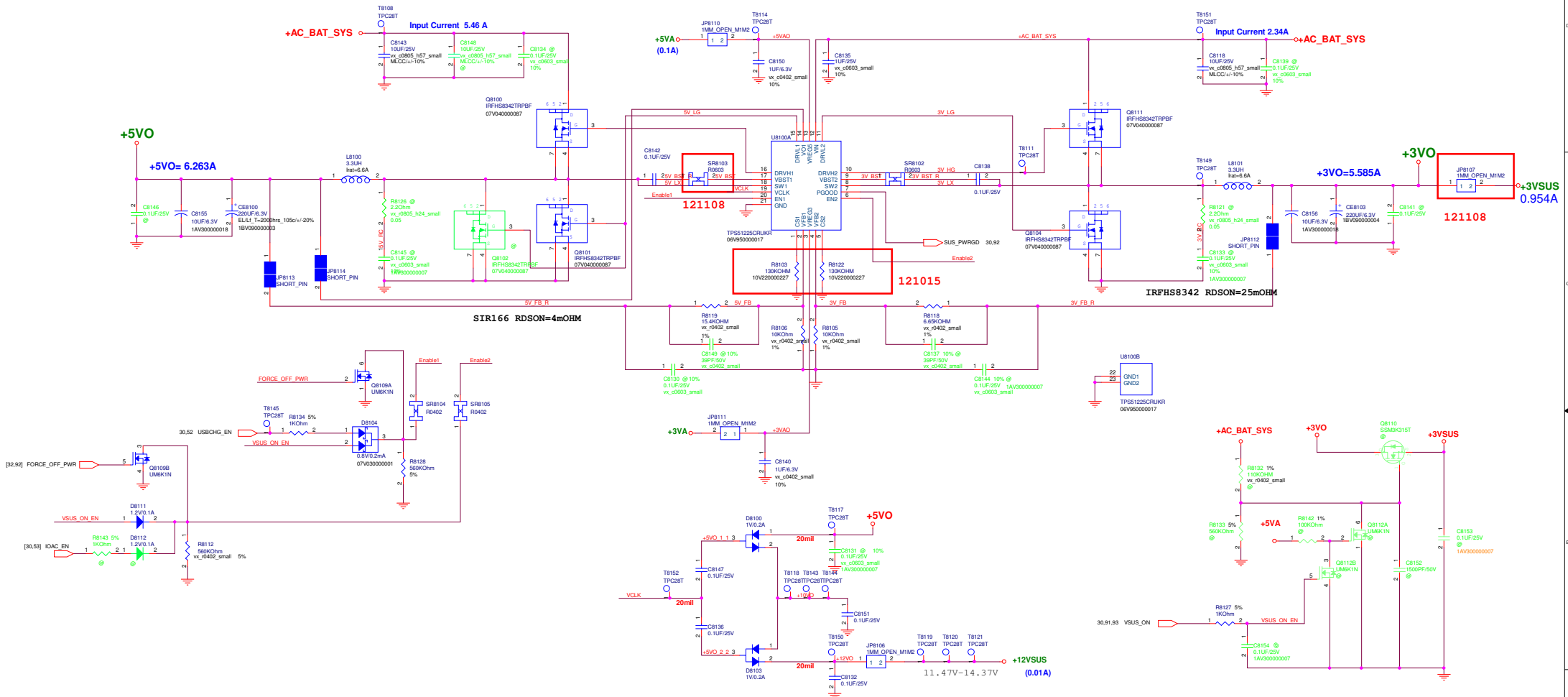
Engineer: Alex

Rev	Project Name	VP70HW	Rev
1	VP70HW	VP70HW	1

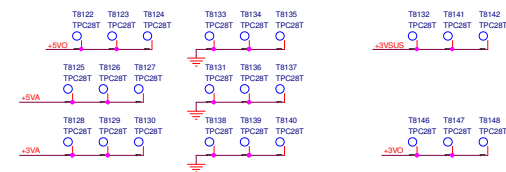
Date: 2019.09.18.2019

Sheet: 30 of 34

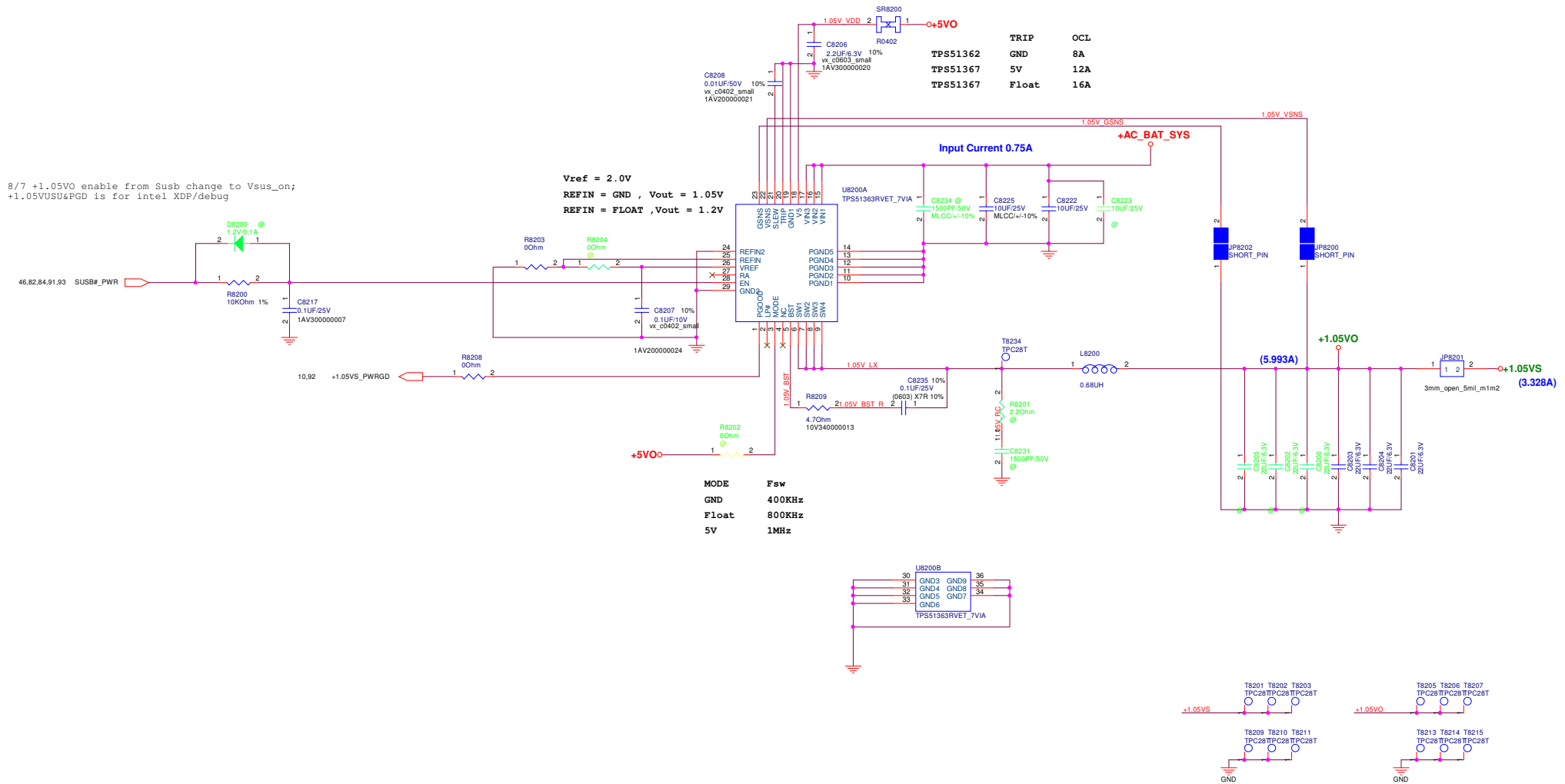
+5VO & +3VO POWER SUPPLY



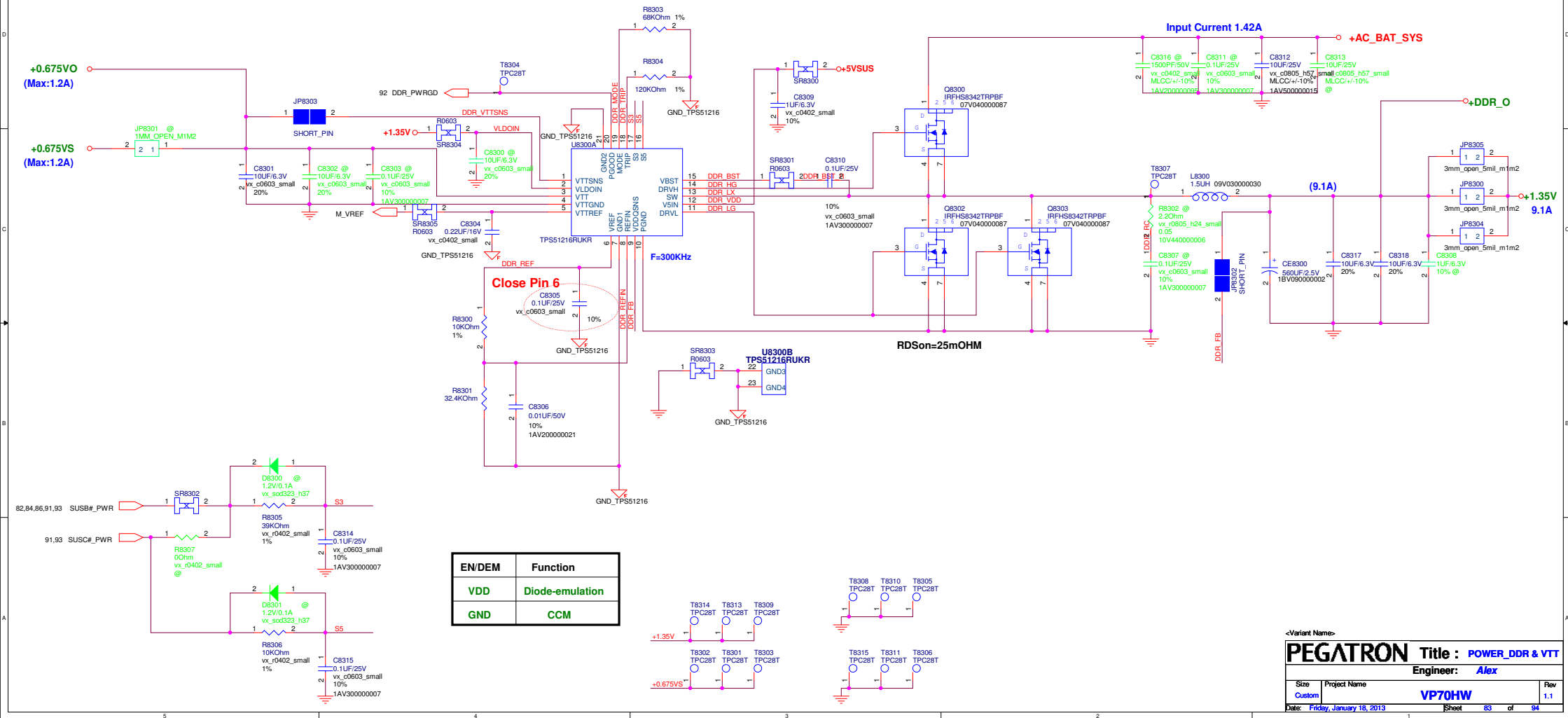
Support ACOC => AOAC_@ 上件 nonAOAC_@ 不上件
nonsupport AOAC => nonAOAC_@ 上件 AOAC_@ 不上件



+1.05VS POWER SUPPLY



DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

PEGATRON Title : POWER_DDR & VTT

Engineer: *Alex*

Size Custom	Project Name VP70HW	Rev 1.1
Date: Friday, January 18, 2013		Sheet 83 of 94

+1.35VS POWER SUPPLY

The schematic illustrates a +1.35V power supply system. Key components include:

- Input Section:** Receives +3VO and +5VA inputs through resistors R8414 and R8415. It features a fuse D8400 and a clamp diode D8401.
- Vref Divider:** A precision resistor network (R8408) sets the reference voltage. Calculations show $V_{ref} = 2.0V$, $R_{EFIN} = GND$, $V_{out} = 1.05V$, and $R_{EFIN} = FLOAT$, $V_{out} = 1.2V$.
- DC-DC Converter:** Utilizes the TPS51362 IC to step down the input voltage. Operating parameters are listed as Input Current 0.94A, MODE GND, Fsw 400KHz, Float 800KHz, and 5V 1MHz.
- Output Filter:** Consists of several electrolytic capacitors (C8409-C8415) and a ferrite bead L8400 to filter the +1.35VS_VGA output.
- Protection:** Includes thermal shutdown pins (TPC28T) connected to JP8400 and JP8402, and a TRIP pin connected to OCL.
- Additional Outputs:** The circuit also provides +1.5VS_LDO and +1.5VS outputs via separate regulators (U8401).

Component Values and Part Numbers:

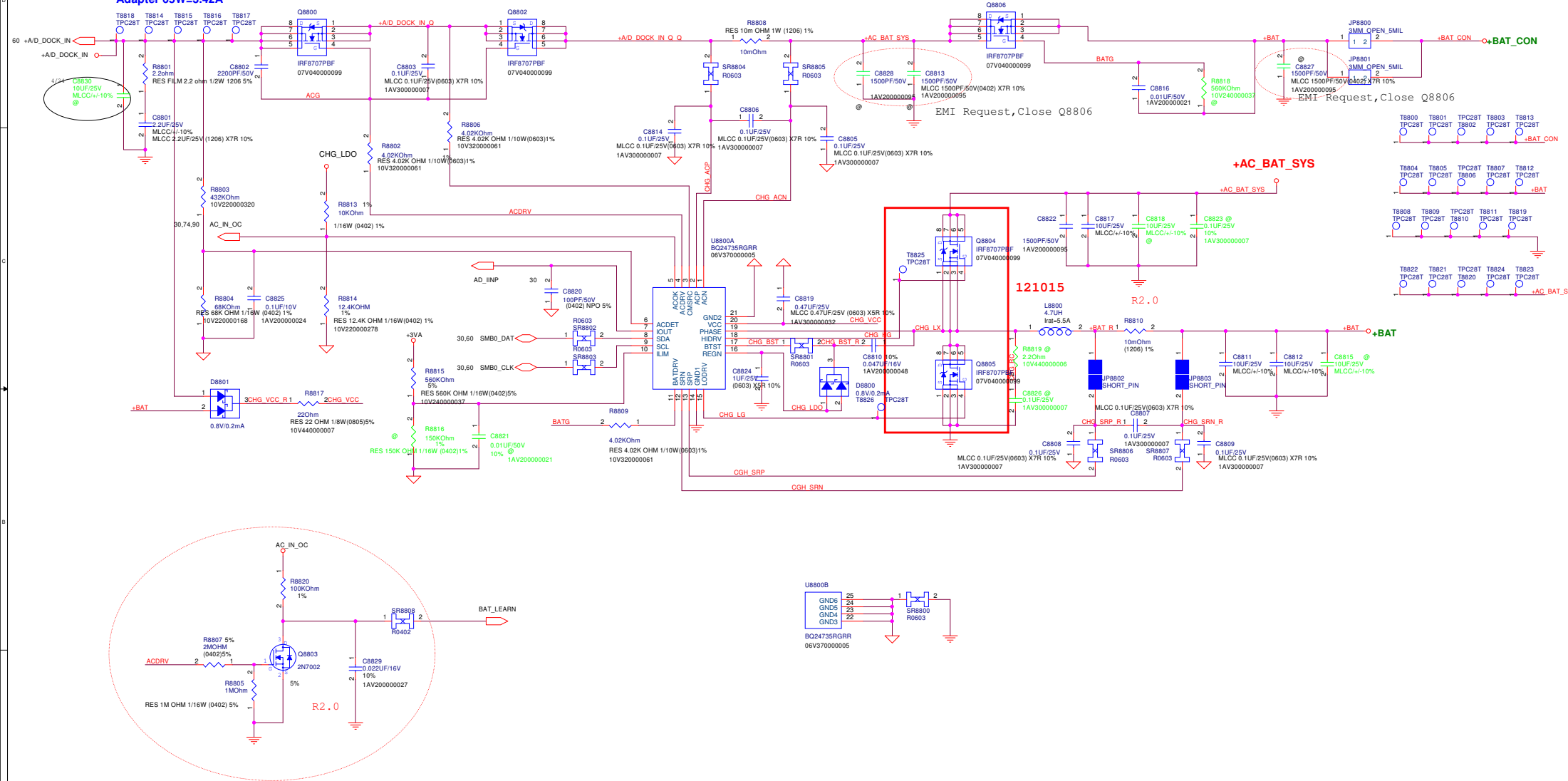
- Resistors: R8414 (82K), R8415 (560K), R8408 (10V220000008, 47.5K), R8411 (0Ω), R8412 (10.5K), R8413 (2.2Ω), R8414 (82K), R8415 (560K), R8416 (560K), R8417 (10V220000007), R8418 (10V220000007), R8419 (10V220000007), R8420 (10V220000007), R8421 (10V220000007), R8422 (10V220000007), R8423 (10V220000007), R8424 (10V220000007), R8425 (10V220000007), R8426 (10V220000007), R8427 (10V220000007), R8428 (10V220000007), R8429 (10V220000007), R8430 (10V220000007), R8431 (10V220000007), R8432 (10V220000007), R8433 (10V220000007), R8434 (10V220000007), R8435 (10V220000007), R8436 (10V220000007), R8437 (10V220000007), R8438 (10V220000007), R8439 (10V220000007), R8440 (10V220000007), R8441 (10V220000007), R8442 (10V220000007), R8443 (10V220000007), R8444 (10V220000007), R8445 (10V220000007), R8446 (10V220000007), R8447 (10V220000007), R8448 (10V220000007), R8449 (10V220000007), R8450 (10V220000007), R8451 (10V220000007), R8452 (10V220000007), R8453 (10V220000007), R8454 (10V220000007), R8455 (10V220000007), R8456 (10V220000007), R8457 (10V220000007), R8458 (10V220000007), R8459 (10V220000007), R8460 (10V220000007), R8461 (10V220000007), R8462 (10V220000007), R8463 (10V220000007), R8464 (10V220000007), R8465 (10V220000007), R8466 (10V220000007), R8467 (10V220000007), R8468 (10V220000007), R8469 (10V220000007), R8470 (10V220000007), R8471 (10V220000007), R8472 (10V220000007), R8473 (10V220000007), R8474 (10V220000007), R8475 (10V220000007), R8476 (10V220000007), R8477 (10V220000007), R8478 (10V220000007), R8479 (10V220000007), R8480 (10V220000007), R8481 (10V220000007), R8482 (10V220000007), R8483 (10V220000007), R8484 (10V220000007), R8485 (10V220000007), R8486 (10V220000007), R8487 (10V220000007), R8488 (10V220000007), R8489 (10V220000007), R8490 (10V220000007), R8491 (10V220000007), R8492 (10V220000007), R8493 (10V220000007), R8494 (10V220000007), R8495 (10V220000007), R8496 (10V220000007), R8497 (10V220000007), R8498 (10V220000007), R8499 (10V220000007), R8500 (10V220000007), R8501 (10V220000007), R8502 (10V220000007), R8503 (10V220000007), R8504 (10V220000007), R8505 (10V220000007), R8506 (10V220000007), R8507 (10V220000007), R8508 (10V220000007), R8509 (10V220000007), R8510 (10V220000007), R8511 (10V220000007), R8512 (10V220000007), R8513 (10V220000007), R8514 (10V220000007), R8515 (10V220000007), R8516 (10V220000007), R8517 (10V220000007), R8518 (10V220000007), R8519 (10V220000007), R8520 (10V220000007), R8521 (10V220000007), R8522 (10V220000007), R8523 (10V220000007), R8524 (10V220000007), R8525 (10V220000007), R8526 (10V220000007), R8527 (10V220000007), R8528 (10V220000007), R8529 (10V220000007), R8530 (10V220000007), R8531 (10V220000007), R8532 (10V220000007), R8533 (10V220000007), R8534 (10V220000007), R8535 (10V220000007), R8536 (10V220000007), R8537 (10V220000007), R8538 (10V220000007), R8539 (10V220000007), R8540 (10V220000007), R8541 (10V220000007), R8542 (10V220000007), R8543 (10V220000007), R8544 (10V220000007), R8545 (10V220000007), R8546 (10V220000007), R8547 (10V220000007), R8548 (10V220000007), R8549 (10V220000007), R8550 (10V220000007), R8551 (10V220000007), R8552 (10V220000007), R8553 (10V220000007), R8554 (10V220000007), R8555 (10V220000007), R8556 (10V220000007), R8557 (10V220000007), R8558 (10V220000007), R8559 (10V220000007), R8560 (10V220000007), R8561 (10V220000007), R8562 (10V220000007), R8563 (10V220000007), R8564 (10V220000007), R8565 (10V220000007), R8566 (10V220000007), R8567 (10V220000007), R8568 (10V220000007), R8569 (10V220000007), R8570 (10V220000007), R8571 (10V220000007), R8572 (10V220000007), R8573 (10V220000007), R8574 (10V220000007), R8575 (10V220000007), R8576 (10V220000007), R8577 (10V220000007), R8578 (10V220000007), R8579 (10V220000007), R8580 (10V220000007), R8581 (10V220000007), R8582 (10V220000007), R8583 (10V220000007), R8584 (10V220000007), R8585 (10V220000007), R8586 (10V220000007), R8587 (10V220000007), R8588 (10V220000007), R8589 (10V220000007), R8590 (10V220000007), R8591 (10V220000007), R8592 (10V220000007), R8593 (10V220000007), R8594 (10V220000007), R8595 (10V220000007), R8596 (10V220000007), R8597 (10V220000007), R8598 (10V220000007), R8599

Date: Friday, January 18, 2013 Sheet 84 of 94

[illegible][illegible][illegible]

BATTERY CHARGER

Adapter 120W=6.32A
Adapter 90W=4.74A
Adapter 65W=3.42A

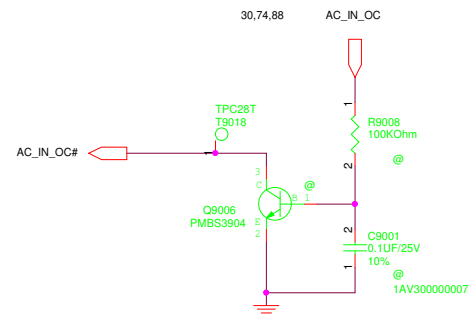
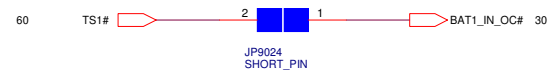


<Variant Name>

PEGATRON Title : POWER_CHARGER			
Engineer: Alex			
Size	Project Name	VP70HW	Rev
Custom			1.1
Date: Friday, January 18, 2013		Sheet 88 of 15	

ADAPTER IN DETECT

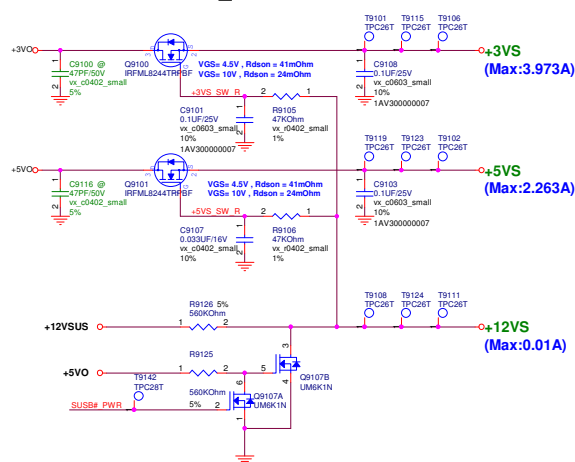
BATTERY IN DETECT



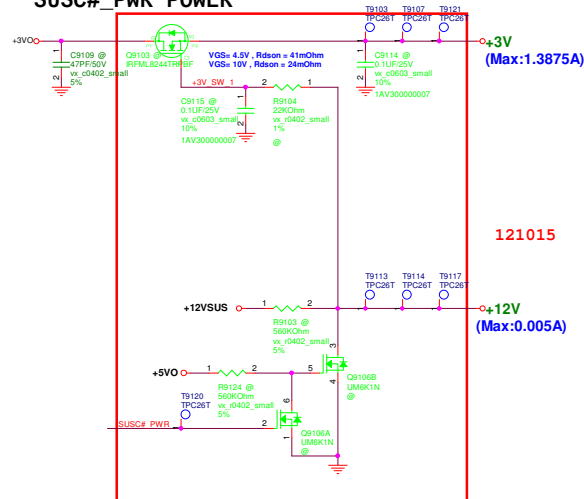
<Variant Name>

PEGATRON Title : POWER_DETECT		
Engineer: Alex		
Size Custom	Project Name VP70HW	Rev 1.1
Date: Friday, January 18, 2013	Sheet 90 of 99	

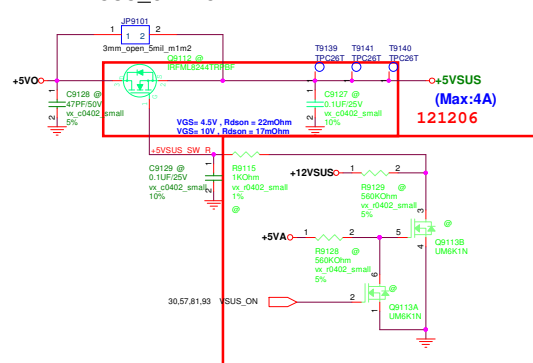
SUSB#_PWR POWER



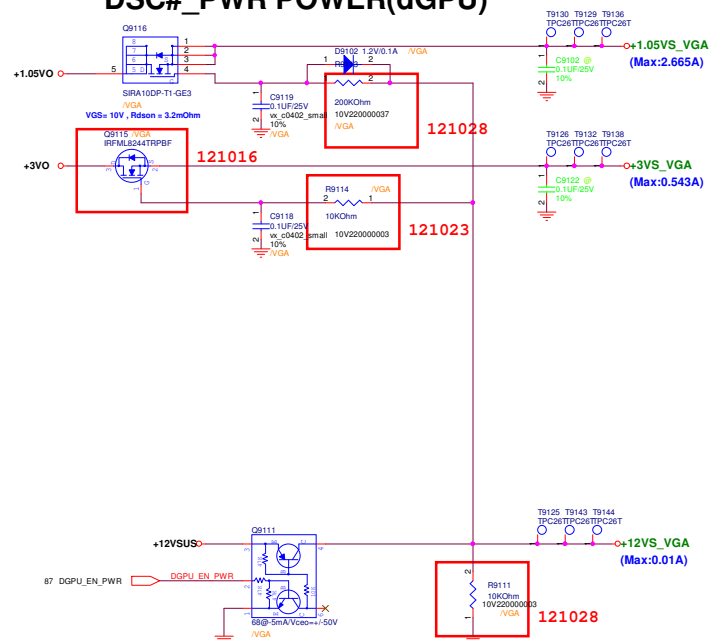
SUSC#_PWR POWER



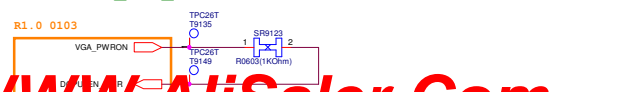
VSUS_ON POWER



DSC#_PWR POWER(dGPU)



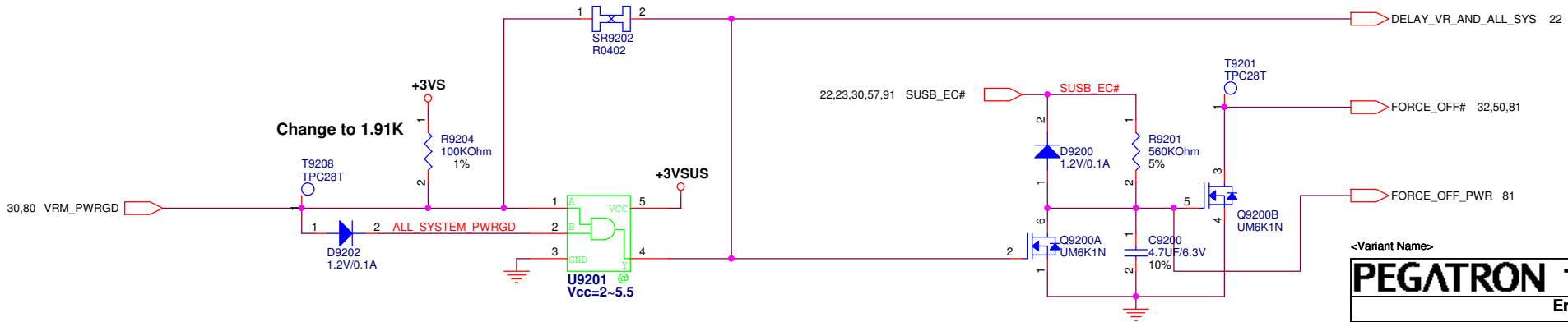
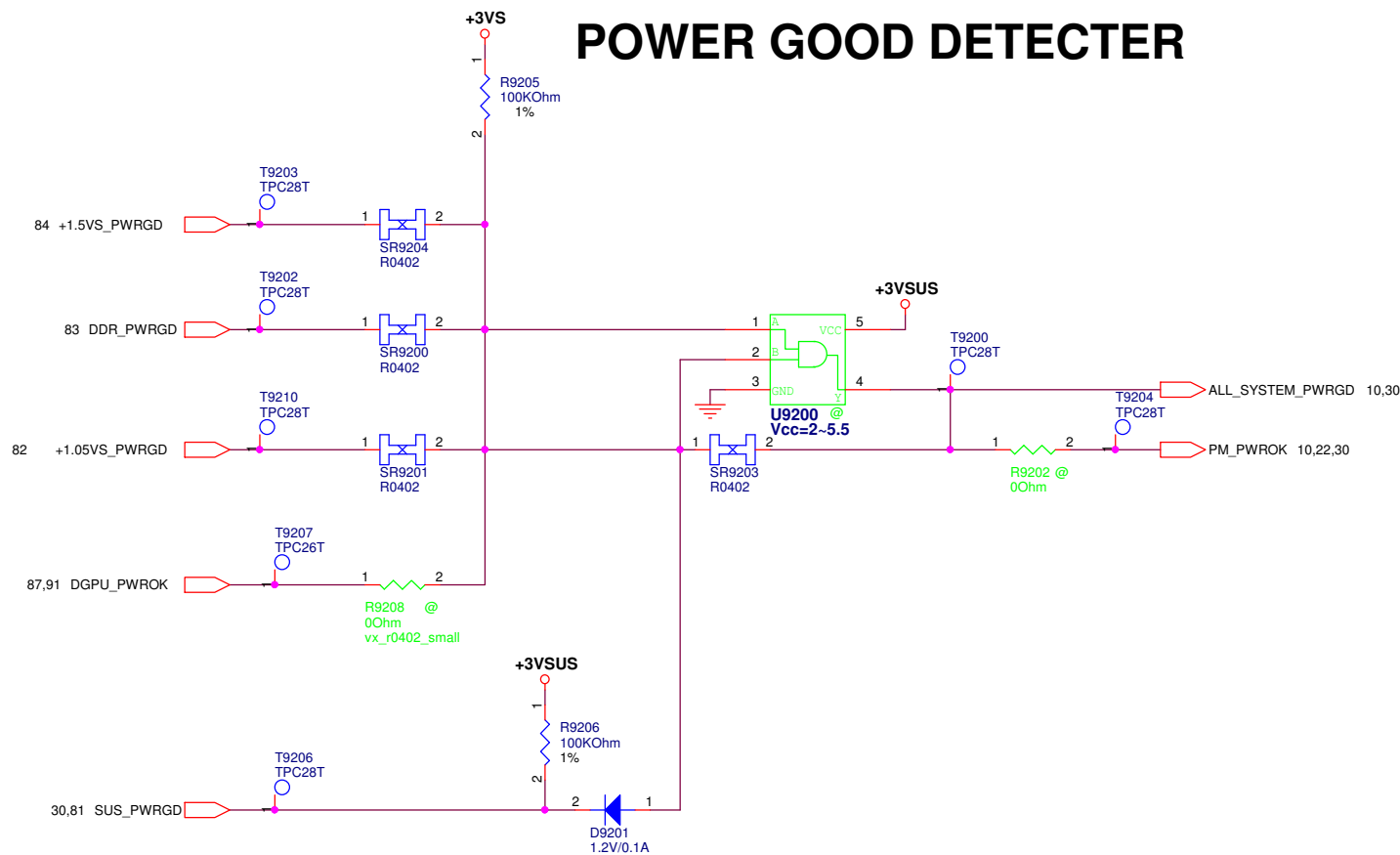
DSC_VGA_PWR POWER Control



<Variant Name>

PEGATRON		Title : POWER_LOAD SWITCH	
Size		Engineer: Alex	
Project Name		VP70HW	
Date: Friday, January 18, 2013		Rev 1.1	
Sheet		91 of 84	

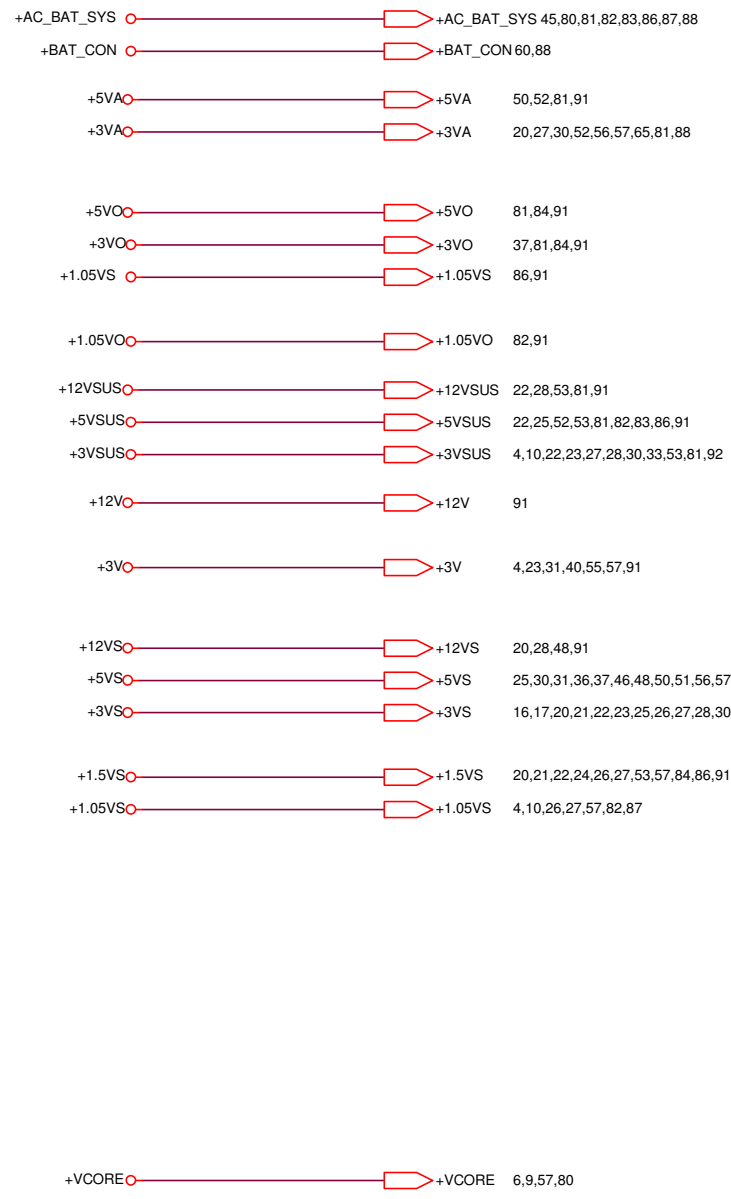
POWER GOOD DETECTER



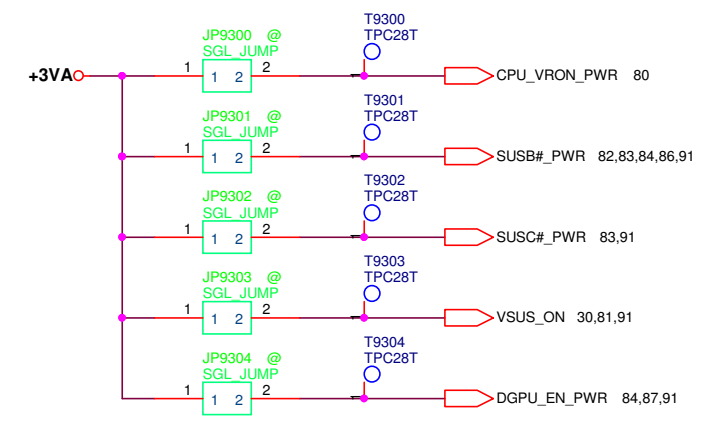
<Variant Name>

PEGATRON Title : **POWER_PROTECT**
Engineer: **Alex**

Size Custom	Project Name VP70HW	Rev 1.1
Date: Friday, January 18, 2013	Sheet 92	of 94



FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Alex	
Size Custom	Project Name VP70HW		Rev 1.1
Date: Friday, January 18, 2013		Sheet 93 of 94	